Self Service Personality Module and Serial Distributed Control Link

Chapter 2.3

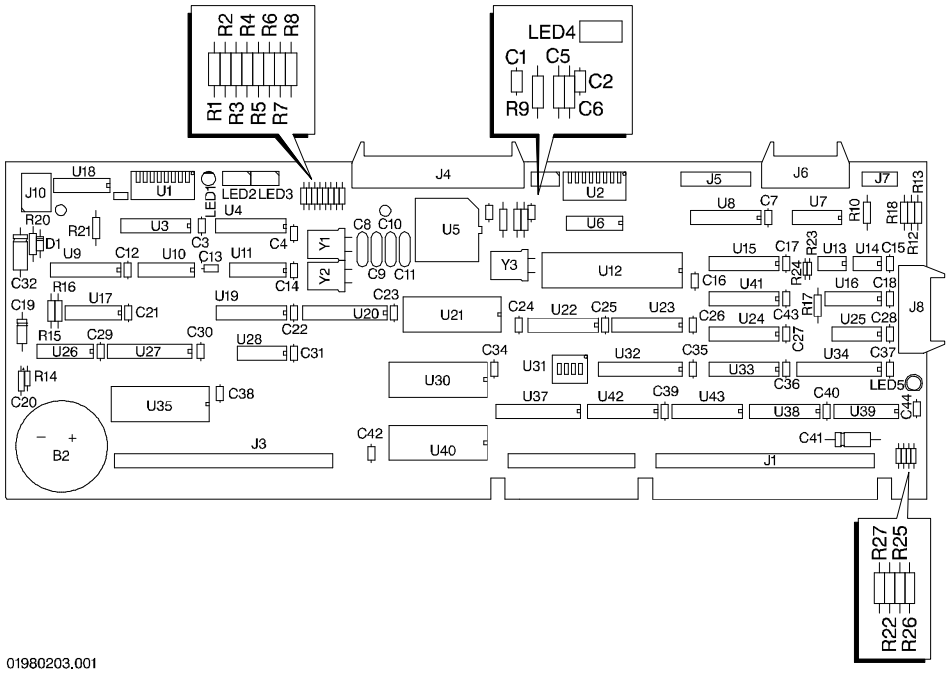
Chapter 2.3

Self Service Personality Module and Serial Distributed Control Link

GENERAL DESCRIPTION

This chapter describes the Self Service Personality Module (SSPM) and the operation of the Serial Distributed Control (SDC) link.

SELF SERVICE PERSONALITY MODULE



01980203.001

The Self Service Personality Module is a single PC expansion card which forms part of the PC core of the NCR 56XX Self Service Financial Terminals.

The purpose of the SSPM is to support the following functional elements:

- SDC master node
- PC compatible flex disk interface
- Battery backed static RAM (NVRAM) for main system storage and security information
- Interface for memory expansion piggy-back module
- Interface for graphics adapter (EGA or VGA) piggy-back modules
- PC level 0 diagnostic/supervisor switch interface
- Extended ROM BIOS diagnostics indicator
- SDC level 0 diagnostics
- Software controlled reset capable of initializing the SDC master node and all connected secondary nodes
- Hard reset for all of PC core.

SDC MASTER NODE

The SDC master node is an intelligent module, comprising both hardware and firmware, which provides an interface between the PC bus and the SDC link. The SDC master node firmware is responsible for achieving features such as; priority based polling, error recovery on the link, and segmenting messages into message blocks.

The hardware components of the master node are:

- Intel 8032 microcontroller
- 64 Kilobytes (KB) of EPROM
- 64 Kilobytes (KB) of SRAM which can be NVRAM to store state-of-health data.

FLEX DISK INTERFACE

The flex disk interface on the SSPM is compatible with NCR ROM BIOS (Version 4.42 and upwards).

NON-VOLATILE RAM

The SSPM provides a block of 24 KB of battery backed system static RAM (NVRAM). This memory is accessed directly from the PC bus and can be selected by software to appear in one of three predefined areas in the PC memory map. Eight KB of security NVRAM is also provided by the SSPM and is accessed directly from the PC bus. The security NVRAM can be selected by software to appear in one of three predefined areas in the PC memory map. The three selectable areas are different from those of the system NVRAM.

MEMORY EXPANSION MODULE

The SSPM has a 62-way connector and mounting holes for use with NCR 1 MB and 4 MB memory expansion piggy-back modules. The signals for this interface are taken directly from the PC bus.

GRAPHICS ADAPTER

The SSPM has a 62-way connector and mounting holes for use with NCR EGA and VGA piggy-back modules. The signals on this interface are taken directly from the PC bus.

NOTE: If the EGA piggy-back option is used, the SSPM requires the space of two adjacent 0.8 in. slots or a single 1.0 in. slot on the PC busboard.

PC LEVEL 0 DIAGNOSTICS INTERFACE

A set of LEDs (1 to 8) on the SSPM displays the codes of the host CPU level 0 diagnostics.

EXTENDED ROM BIOS DIAGNOSTICS (STATE OF HEALTH) INDICATOR

A bicolour LED, 14 (shown as LED assembly number 5 on the board screen printing and on the schematic) on the SSPM indicates the state of health of the PC core. The PC core extended ROM BIOS diagnostics resets and interrogates each of the eight port addresses used by intelligent boards. From power-up LED 14 glows red. If all the ports have been interrogated and no errors have been found then LED 14 is turned green to indicate that the PC core is healthy. If errors are detected the LED remains red and the error condition is displayed on the LEDs 1 to 8 of the SSPM (refer to Chapter 2.2 for a description of the error codes displayed).

NOTE: Number 14 is used for the bicolour LED in this description to distinguish it from LED 5 in the bank of PC level 0 LEDs.

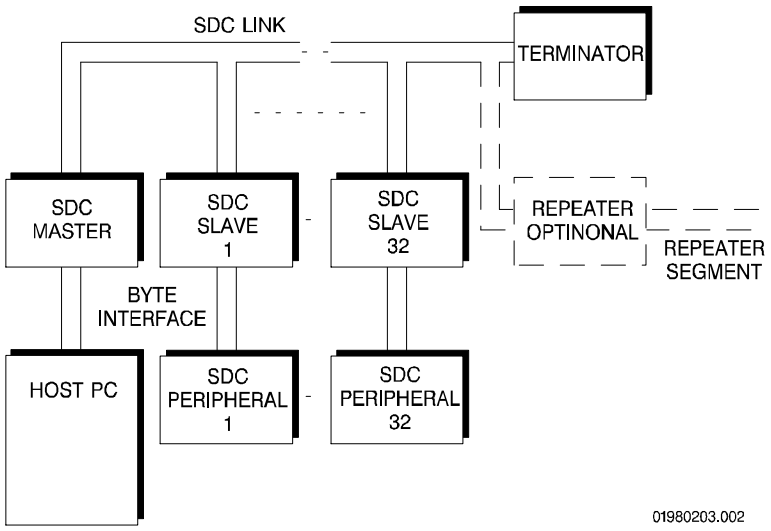
SDC LEVEL 0 DIAGNOSTICS

LEDs (10 to 13) and switches (9 to 16) on the SSPM permit selected level 0 tests to be carried out on the SDC master node hardware.

HARD RESET

The host PC (the Processor Board) can issue a reset to the PC core by writing to an I/O port.

SERIAL DISTRIBUTED CONTROL LINK



The SDC link is a serial multidrop link which permits the exchange of commands and data between a primary (master) node and a number of intelligent secondary (slave) nodes. Up to 32 physical devices may reside on the SDC link, each having one of 128 possible logical link addresses. The purpose of the link is to provide an expansion system:

- which is not limited by the host's address capacity
- in which added peripherals do not impact on the host's memory
- with simple wiring
- which can be used to connect the host processor to modules within close physical proximity
- provides high performance of peripherals
- has distributed intelligence.

The operation of the link is based on the Intel 8032 microcontroller using the 11 bit “wake up” feature (start bit, eight data bits, address/data flag bit, and stop bit). All the secondary devices on the SDC link wake up when they receive a byte with the address bit set to “1”. On receipt of the address byte, each secondary device compares it with its own address and, if it does not match, it ignores the rest of the message. If the address is correct for that device, then the secondary will process the message. The handling of this protocol is done by the 8032 microcontroller.

Characteristics of the link protocol are:

- Each link address can have 8 associated device numbers
- The maximum number of secondary addresses is 127 (1-127)
- Data transmission is asynchronous, two-way alternate (half-duplex)
- Data transmitted is binary
- Transmission speed is 187 500 bits/second
- There are no special hexadecimal characters; the link protocol provides complete data transparency for the information on the line
- Data transfer is segmented if necessary into 64 byte blocks
- The SDC master is always in control of the messages on the SDC link.

The hardware components of the SDC link are:

- Master node
- Slave node interfaces
- Repeater node
- Interconnect cabling.

MASTER NODE

The SDC master node is located on the SSPM.

SLAVE NODE INTERFACES

The slave node interfaces are located on each of the SDC module interface boards. The hardware of a slave node includes:

- Intel 8032 processor
- RS485 transceivers
- EPROM containing level 0 diagnostics and SDC slave node link interface firmware
- SRAM containing the downloaded device firmware and data.

Devices which are operated via slave nodes include:

- the printers
- the touch screen
- the MSR/MCRW
- the videodisc player
- the keyboards.

The operation of a slave node is described only in this chapter and will not be repeated in the chapters for the individual modules.

SDC1 and SDC2

On SDC1 devices the software which is the device driver is downloaded from the hard disk to RAM on the driver board local to the device and the communications driver is contained in ROM on the board. With SDC2 devices both software drivers (device and communications) are downloaded to the driver board. The software which handles the download is known as the Self Service Systems Software (abbreviated to S4). SDC2 devices operate with S4 release 4 and above.

REPEATER NODES

The link architecture supports repeater nodes which are used to increase the length of the link for the connection of remote devices. A repeater appears, electrically, to be a normal node to the master segment; the repeater transceiver circuits are controlled by the currently active slave device so that the repeater function is transparent to the master.

Devices (up to 32) which are able to connect to a repeater segment must generate the transceiver enable signal. Also devices on segments outside the host terminal must have signal grounds connected to the signal reference wire via a 100 ohm resistor.

The repeater segment is terminated at each end via a 110 ohm resistor on each signal pair.

The maximum total cable length without using repeaters is 300 metres.

INTERCONNECT CABLING

The signals on the SDC bus conform to the EIA RS485 standard (balanced digital multiple point system) and consist of three differential signals DATA, RESET, and TXEN and one reference ground GND. Within the terminal, each differential signal is carried on a stranded twisted wire pair of characteristic impedance 100-120 ohms. The data signal pair TXEN is terminated at each end via 110 ohm resistors and the data signal pair DATA is biased on the SSPM using 220 ohm resistors and is terminated at the remote end by a 110 ohm resistor. Short sections of flat ribbon cable occur at intervals on the stranded wire cable to permit the attachment of 10-pin (dual five) type connectors.

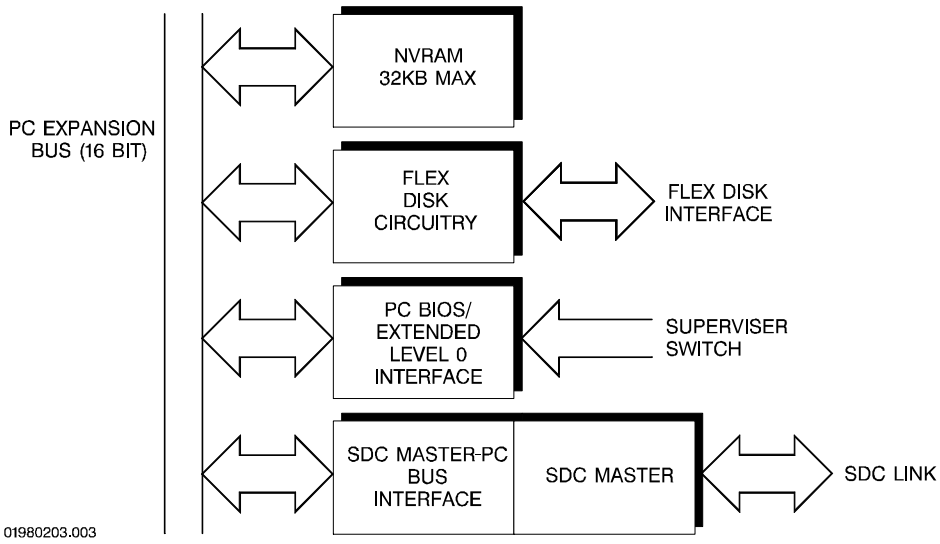
Cables outside the terminal must be screened.

The physical topology of the SDC link is that of a daisy chain correctly terminated at both ends. This arrangement applies to the master segment and any repeater segments. The link master is the first device on the master segment and a repeater segment may be placed at any point on the master or on another repeater segment.

THEORY OF OPERATION

This section provides an overview of the operation of the SSPM and SDC link.

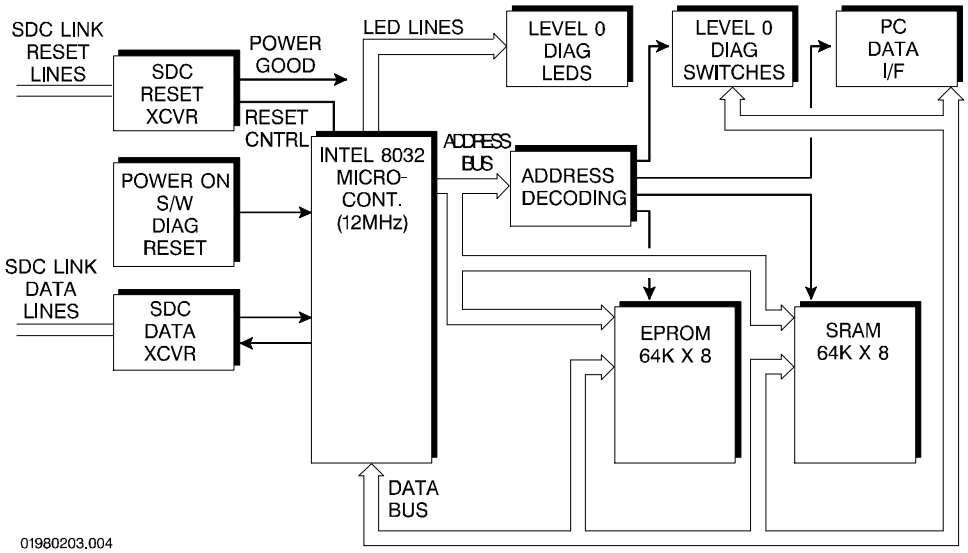
SELF SERVICE PERSONALITY MODULE



The SSPM printed circuit board operation is described under the following functional headings (refer to the schematic diagram for the SSPM, pages FO - 1 or FO - 9):

- SDC Master
- PC Bus Interface
- Flex Disk Interface
- Non-Volatile RAM
- PC Level 0 Diagnostic Interface
- Graphics Adapter
- Memory Expansion.

SDC MASTER



The SSPM houses the Serial Distributed Control (SDC) Master for the SDC link architecture. A master/slave scheme is implemented with each of the slaves being polled by the master.

8032 Processing Element

An 8032 microcontroller running at 12MHz is used as the main processing element. An external crystal and internal oscillator provide the clock source.

The 8032 has four onboard 8-bit I/O ports which are designated as follows:

Port	Function
P0.0-P0.7	Multiplexed Address/Data Bus, AD0-7
P1.0-P1.3	LED Indicators 0-3
P1.4	No connection
P1.5	RESET in enable, RES_IN_EN
P1.6	RESET out enable, RES_OUT_EN/
P1.7	TRANSMIT enable, TX_EN/
P2.0-P2.7	Upper Address Bus, A8-15
P3.0	Serial data input, RXD
P3.1	Serial data output, TXD
P3.2	External Interrupt 0, SDC_BUFF_FULL/
P3.3	External Interrupt 1, PC_BUFF_FULL/
P3.4	No connection
P3.5	No connection
P3.6	External Data memory write strobe, WR/
P3.7	External Data memory read strobe, RD/

All reserved ports power-up driving a logic “1”

Where,

- ALE (Address Latch Enable) is the output pulse for latching the low byte of the address during access to external memory
- /PSEN (Program Store ENable) is the read strobe to external program memory (EPROM only on the SDC master)
- /EA is the external memory access pin and is tied low, forcing all program memory fetches to be external.

Memory

The 8032 memory consists of code and data space. Code address space consists of a single EPROM socket which can accept a 64K device and is populated from 0000H upwards. Data space consists of two 32K SRAM devices populated from 0000H upwards. The area from 0000H-00FFH is used by iDCX data and that from 3E00H-3FFFH is designated as memory mapped I/O, and so neither can be used for general purpose data storage.

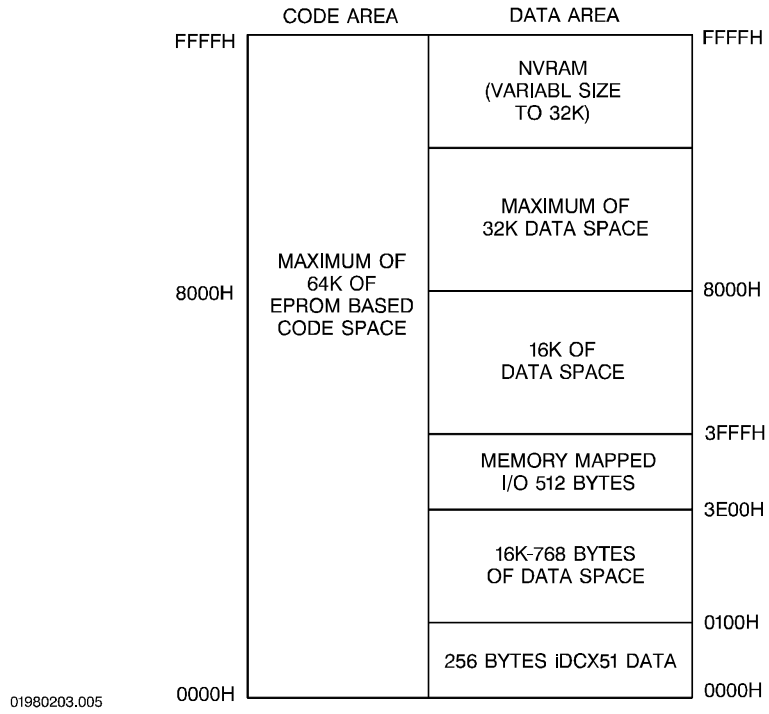
The top 32K SRAM is battery backed-up using the same battery and voltage supervisor device as used for System NVRAM. Although the entire physical device is battery backed-up only a part of it may actually be defined as NVRAM. On reset, execution of the code starts at 0000. Level 0 diagnostics, iDCX-51 core, Bus I/F firmware and SDC master link firmware all reside within the code area.

The memory control signals for program and data memory are as follows:

Signal Function	Signal Name	Decode
EPROM select	GND	Always selected - this is implemented by allowing a pull-up resistor to be put through an inverter for test purposes
EPROM read	/PSEN	
SRAMH select	/CE	Controlled from the Voltage Supervisor Device
SRAMH read		BA15./(/RD)
SRAHM write		BA15./(/WR)
SRAML select		/BA15.BA14 + /BA15./BA14./BA13 + /BA15./BA14./BA12 + /BA15./BA14./BA11 + /BA15./BA14./BA10 + /BA15./BA14./BA9
SRAML read	/RD	
SRAML write	/WR	

NOTE: EPROMs should have access times of 200ns or less, SRAMs should have access time of 120ns or less.

8032 Memory Map



Memory Mapped I/O

Memory mapped I/O is located in the data area between addresses 3E00H-3FFFH.

The following ports exist in this area of memory:

Port	Location (HEX)	W/R	Description
SDC Level 0 switches	03FF8	R	Reads the configuration of the level 0 switches

NOTE: The level 0 configuration switches are switches 9-16 the byte read back defining them as:

Data Bit	Function	
0	SWITCH 9	
1	SWITCH 10	
2	SWITCH 11	0 - Switch Open
3	SWITCH 12	1 - Switch Closed
4	SWITCH 13	
5	SWITCH 14	
6	SWITCH 15	
7	SWITCH 16	

Port	Location (HEX)	W/R	Description
Bus Interface Status	03FF0	R	Reads the status of the single byte buffer between the host PC and the SDC master controller.
	(03FE0 (	R/W	Reads data from/Writes data to the host PC via the single byte buffer.
BUS Interface Data Ports	(03FE1 (	R/W	Reads commands from/Writes commands to, the host PC via the single byte buffer.
	(03FE2	W	Writes error statuses to the host PC.
PC Interrupt Line Selection	03FD0H	W	Sets the interrupt line used by the PC-SDC master bus interface to the PC

SDC LINK INTERFACE

The SDC link interface on the SDC master node consists of the following sections:

- Data Lines:
  - Incoming data on the SDC link differential data lines DATA+ and DATA- is converted to TTL levels by a SN75176 transceiver device and then goes to the receive data line (Port 3.0) on the 8032 microprocessor. Reception of data is always enabled by hardware.
  - Data being transmitted by the 8032 microprocessor (Port 3.1) is converted by the same SN75176 transceiver device to the necessary RS485 levels on the DATA+ and DATA- lines. Data will only reach the DATA+ and DATA- lines if the transmitter enable signal (/TX_EN) is active (Port 1.7 = 0). When transmission occurs, the transmitted data is echoed back to the receive pin of the 8032. For this reason, receive interrupts on the 8032 are disabled when transmission is about to occur.
  - The data lines are defined to be in a mark (logic 1) state by means of 220 ohm biasing resistors pulling DATA+ to +5V and DATA- to ground. Thus, when there is no node (primary or secondary) driving the lines, the differential lines will remain in a known (logic 1) state.
- Reset Lines:
  - The differential reset lines, RESET+ and RESET-, are normally defined to be in a non-reset state (logic 0) by means of 220 ohm biasing resistors pulling RESET+ to ground and RESET- to +5V. If the SSPM wishes to drive the reset active it enables the reset-out signal (/RESET_OUT_EN = 0) which automatically drives the differential reset lines active. When doing this the SSPM disables the reset-in signal (RESET_IN_EN = 0) so that the reset will not be fed back to the PC Core.
  - A device on the SDC link may have the capability to drive the differential reset lines. The SSPM enables the reset for input by setting the reset-in signal (RESET_IN_EN = 1). Thus if the reset lines are driven active the reset will be allowed through the reset transceiver device to the POWER_GOOD signal. The POWER_GOOD signal will be driven low which will reset the entire PC Core until the reset by the SDC device is released.
  - The reset lines are not terminated due to the fact they are static signals.

- Transmit Enable Line - Although the differential transmit enable lines, TX_EN+ and TX_EN-, are driven only by secondary SDC nodes and used only on a repeater segment of the SDC link, the signals are terminated by a 110 ohm resistor on the SDC master to allow the use of exactly the same SDC secondary nodes on the main SDC link section
- Signal Reference Line - the signal reference connection is a ground connection via a 110 ohm resistor on the SDC master node.

SDC LEVEL 0 DIAGNOSTICS

The SDC master reads specific test codes from the switches at port 03FF8H and displays test results on the four LEDs 10-13, at 8032 ports P1.0-P1.3. A logic “1” turns the LEDs on, a logic “0” switches them off.

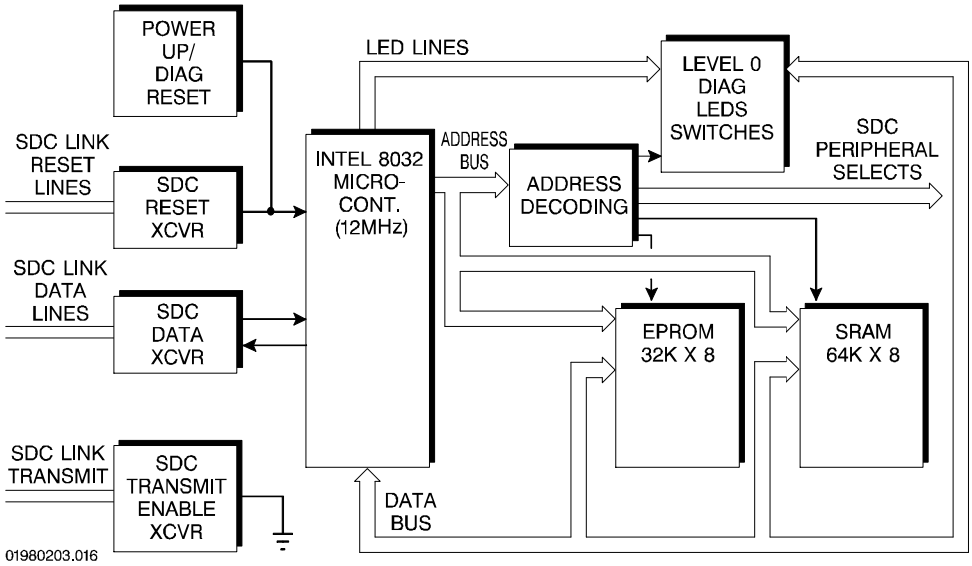
Level 0 diagnostics exercises ROM, RAM, the 8032 Microcontroller, and an internal turnaround test on the SDC link interface can also be selected.

Level 0 diagnostics also handles the initial setup and communication with the PC via the byte interface. It allows the passing of board identification data to the PC and will also setup the interrupt line used by the PC-SDC Bus Interface back to the PC.

Signals from the level 0 switches and from LEDs 10-13 are available on an external test connector, J6, and additionally a reset line is available at the connector to allow an external test device to drive the SDC master in the same way that it would be driven from power-up. In this case the onboard switches must all be open.

For a description of level 0 diagnostic switch settings and result codes see the section “Service Aids - Level 0 Diagnostics”.

PC BUS INTERFACE



The SDC master communicates with its host PC via a one byte buffer, controlled by several interface flags and/or interrupt lines.

Commands, data, and error statuses are stored in the same physical buffer but are issued at their own specified I/O locations to set/reset the appropriate flags.

Each side of the interface has its own physical buffer so that the SDC master can send data to the PC at the same time as the PC is sending data to the SDC master.

Interface flags control the access to the buffers; each side having its own set of flags. The interface flags can also cause specific interrupts all of which can be masked off.

The I/O locations used for the bus interface on the SDC master side are defined in the section “Memory Mapped I/O”.

To avoid possible conflict with other PC expansion boards, the area of the host PC's I/O space into which the bus interface is mapped can be configured using two switches. The four areas available are:

Switch 18	**Switch 17**	**I/O On Host PC**
closed	closed	0200H - 020FH (Default)
closed	open	0210H - 021FH
open	closed	0300H - 030FH
open	open	0310H - 031FH

NOTE: Throughout this chapter it is assumed that the SSPM bus interface is located in I/O space 0200H - 020FH and the port addresses are, therefore, as shown in the following table.

Port Name	Port	Read/Write	Purpose
PC_DATA_RD	0200H	R	Read data from the SDC master.
PC_DATA_WR	0200H	W	Send data to the SDC master.
PC_CMD_RD	0202H	R	Read commands from the SDC Master
PC_CMD_WR	0202H	W	Send commands to the SDC Master.
PC_ERROR_RD	0200H	R	Read error statuses from the SDC master.
PC_MASK_WR	0204H	W	Set up the allowable interrupt sources to the host PC.
PC_FLAGS_RD	0208H	R	Read the bus interface flags on the host PC side.
PC_S/W_RESET	0208H	W	Allow the host PC to reset the SDC master and the bus interface.
PC_SWITCH_RD	020CH	R	Read PC extension level 0 codes from switches 1-8.
PC_LED_WR	020CH	W	Send PC extended level 0 result codes to LEDs 1-8.
PC-NVRAM_SET	020DH	W	Set up system NVRAM address and size.
SOH_LED	020EH	W	Alter state of health LED.
PC_HARD_RESET	020FH	W	Allow the host PC to reset the PC Core.

Bus Interface Flags

There are five bus interface flags which control access and give information about the PC bus interface. The meanings when set to 0 or 1 are shown in the following table:

Flag	0	1
PC_BUFFER_FULL	Buffer on PC side is empty.	Buffer on PC side has been written to
PC_COMMAND/DATA	Byte in PC buffer is data.	Byte in PC buffer is a command.
SDC_BUFFER_FULL	Buffer on SDC master side is empty.	Buffer on SDC master side has been written to.
S D C _ COMMAND/DATA	Byte in SDC master buffer is data.	Byte in SDC master buffer is a command
SDC_ERROR	SDC master is operating normally.	Error condition from the SDC master

On power-up and any reset condition (see “Reset of the SDC Master”) all the bus interface flags are reset to a 0.

When the host PC or the SDC master enquires about the status of the bus interface it is sent back four of the five flags.

Host PC

When the host PC reads from PC_FLAGS_RD (IN from port 0208H) it accesses all flags except the PC_COMMAND\DATA flag:

Data Bit	Flag
0	SDC_BUFFER_FULL
1	PC_BUFFER_FULL
2	SDC_COMMAND\DATA
3	SDC_ERROR
4	Reserved
5	Reserved
6	Reserved
7	Reserved

SDC Master

When the SDC master reads from SDC_FLAGS_RD (READ from location 03FF0H) it accesses all flags except the SDC_COMMAND\DATA flag:

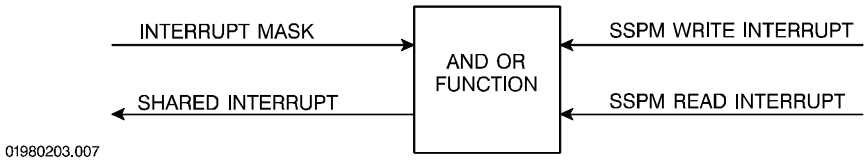
Data Bit	Flag
0	SDC_BUFFER_FULL
1	PC_BUFFER_FULL
2	PC_COMMAND\DATA
3	SDC_ERROR
4	Reserved
5	Reserved
6	Reserved
7	Reserved

Interrupt Structure

Various interrupts are generated by the bus interface to the SDC master and to the host PC.

Interrupts To The Host PC

The diagram shows how two interrupts sources are effectively "ORed" together to form a single shared interrupt line back to the host PC.



These are the flags SDC_BUFFER_FULL and PC_BUFFER_FULL (acting as an inverting PC_BUFFER_EMPTY flag). Thus an interrupt can be returned to the host PC when the SDC master writes data to it (a receive interrupt) or when the SDC master reads the data that the host PC had previously sent (a transmit interrupt).

Either or both of the interrupts can be masked out by the host PC writing to its interrupt mask register (Port 0204H).

The byte written to the mask register is partitioned into mask bits as follows :

Bit	0	1
TRANSMIT MASK		
D0	PC_BUFFER_EMPTY will not cause an interrupt	PC_BUFFER_EMPTY will cause an interrupt
RECEIVE MASK		
D1	SDC_BUFFER_FULL will not cause an interrupt	SDC_BUFFER_FULL will cause an interrupt

The remaining bits D2, D3, D4, D5, D6 and D7 are reserved and should be reset to zero.

The power-up state of both the mask bits is "0." That is both interrupts to the host PC are masked off.

In the case of a PC_BUFFER_EMPTY (transmit) interrupt, the cause of the interrupt will still be active until another byte is sent by the host PC. For this reason the interrupt should be masked off in the Interrupt Service Routine (ISR) until another byte is sent by the PC.

The single shared interrupt line back to the PC will be configured by level 0 diagnostics on the SDC master on reset. The interrupt line to be used will be determined by the host PC and the information passed over the byte interface.

Location	R/W	Description
03FD0H	W	Sets the interrupt line used by the PC-SDC master bus interface to the PC.

Data Bit	Flag
0	INT_SEL_0
1	INT_SEL_1
2	INT_SEL_2
3	}
4	}
5	} Reserved (Should be reset to 0)
6	}
7	}

The 3 least significant bits of the byte can be used to define interrupt lines 2 to 7 back to the PC:

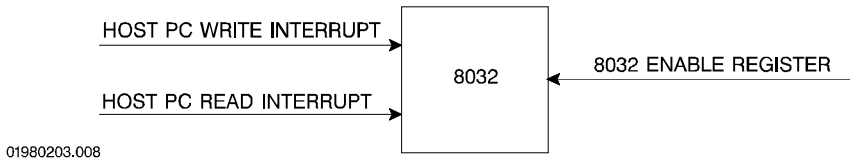
INT_SEL_2	INT_SEL_1	INT_SEL_0	PC INTERRUPT LINE
0	0	0	Reserved
0	0	1	Reserved
0	1	0	IRQ2 (Default)
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6 This is used by the Flex Disk
1	1	1	IRQ7

On power-up and any reset condition the interrupt line selection is reset to 0, that is the interrupt is not allowed back to the PC.

Because two interrupt sources use the same interrupt line, when an interrupt is received from the SDC master the host PC must read its own flags register at PC_STATUS_RD (IN from 0208H) in order to determine the actual source of the interrupt. It is possible for both interrupt sources to be active at the same time, for example if the SDC master reads the byte sent to it by the PC and then sends a response to it before or during the interrupt routine which acts on the read condition. Because the interrupt controller in the PC is edge triggered, the controller will not flag up another interrupt and so the ISR must check for the occurrence of both possible interrupts.

Interrupts To The SDC Master

Both interrupts generated by the bus interface during data transfer go directly to the 8032 Microcontroller on the SDC master. These are, the inverse of PC_BUFFER_FULL, generated when the host PC writes to the single byte buffer, and SDC_BUFFER_FULL (effectively a SDC_BUFFER_EMPTY interrupt), generated when the host PC reads the single byte buffer.



Both or either of the interrupt sources can be masked out by programming the 8032's Interrupt Enable register. In the case of an SDC_BUFFER_EMPTY (transmit) interrupt the cause of the interrupt will still be active until another byte is sent by the SDC master. Thus the interrupt should be disabled by the 8032 in the ISR until another byte is sent.

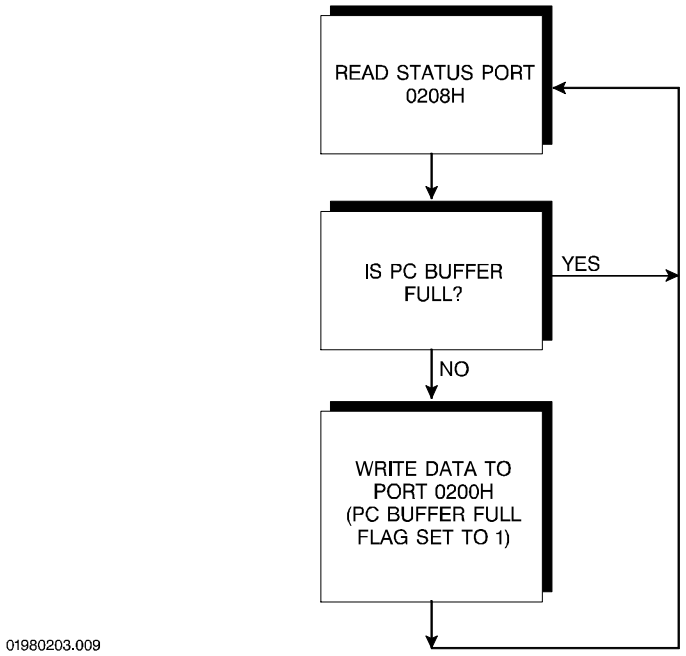
Data Transfer on the PC Bus Interface

Data from the Host PC to SDC Master

Sending data to the SDC master can be either interrupt driven or polled. If it is polled the host PC can transmit only if it finds that PC_BUFFER_FULL = 0 in its own flags register. It will then send data to the single byte buffer and will either have finished its message or be waiting to transmit the next byte.

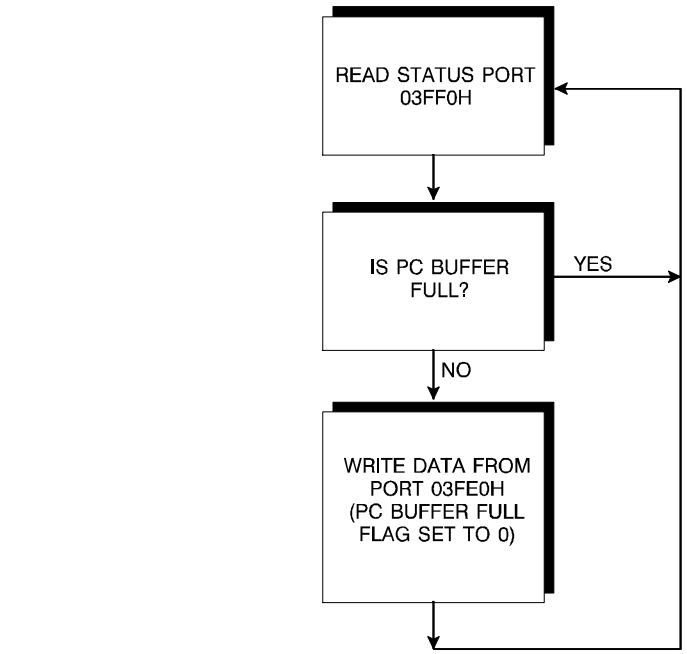
If the message transmission is being interrupt driven the host PC will send data only when it receives a PC_BUFFER_EMPTY interrupt. Once the data is sent it may resume its previous operation.

Host PC Side



Writing data to PC_DATA_WR sets the PC_BUFFER_FULL flag to a “1” and also generates a PC_BUFFER_FULL interrupt to the SDC master.

SDC Side



01980203.010

Reception of data sent from the host PC can also be polled or interrupt driven. If polled then the SDC master waits for PC_BUFFER_FULL = 1 and when this occurs it reads the data from the byte buffer. This then repeats until the entire message has been transmitted across the bus interface.

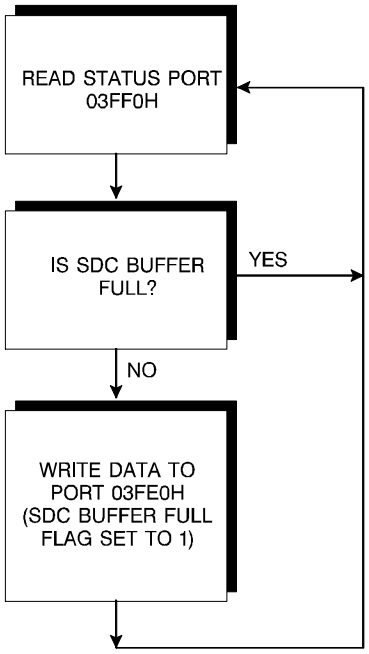
If the reception of data is interrupt driven the data is only read when a PC_BUFFER_FULL interrupt occurs. When the byte has been read in, the previous operation may be resumed.

Reading the data sent by the PC will reset the PC_BUFFER_FULL flag to a “0” and, if the transmit mask is on, will also generate an interrupt to the host PC. The host PC must then read its flags register to determine that the interrupt was a PC_BUFFER_EMPTY interrupt.

Data From The SDC Master To The Host PC

Sending data to the host PC can be either interrupt driven or polled. If it is polled the SDC master can only transmit if it finds that SDC_BUFFER_FULL = 0 in its own flags register. It will then send data to the single byte buffer and will either have finished its message or will be waiting to transmit the next byte. If the message transmission is being interrupt driven the SDC master will only send data when it receives an SDC_BUFFER_EMPTY interrupt. Once the data is sent it may resume its previous operation.

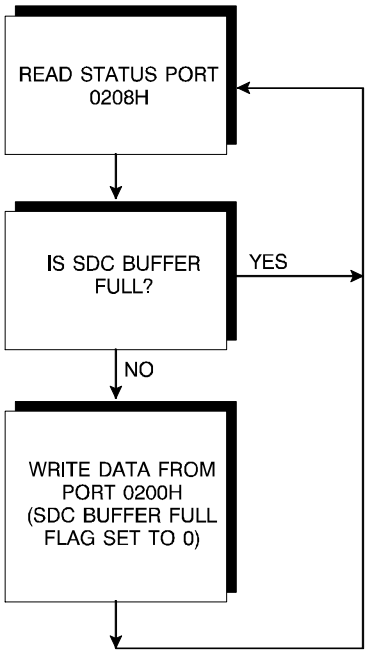
SDC Side



01980203.011

Writing data to SDC_DATA_WR sets the SDC_BUFFER_FULL flag to a "1" and also generates an SDC_BUFFER_FULL interrupt to the host PC.

Host PC Side



01980203.012

Reception of data sent from the SDC master can also be polled or interrupt driven. If polled then the host PC waits for SDC_BUFFER_FULL = 1 and when this occurs it reads the data from the byte buffer. This then repeats until the entire message has been transmitted across the bus interface.

If the reception of data is interrupt driven then the data is read only when an SDC_BUFFER_FULL interrupt occurs. When the byte has been read in, the previous operation may be resumed.

When the host PC reads the single byte buffer, SDC_BUFFER_FULL is reset to a "0" and an SDC_BUFFER_EMPTY interrupt is returned to the SDC master.

Commands From The Host PC To The SDC Master

The following commands may be sent by the SDC service program to the Primary manager

- IDENTIFY MODULE - sent by the service program to ascertain the module configuration block
- IDENTIFY TASK SERVICES - sent by the service program to ascertain which services are supported on the primary node
- RESET_SEQUENCE_NO - sent to the primary manager to reset the sequence numbers on the primary for a secondary node that has been reset by the soft reset command
- DETERMINE_ATTACHMENTS - sent by the service program to ascertain which nodes are physically connected
- SET_SERVICE_PRIORITY - sent by the service program to define the priority, on the communications link, of a specific service
- TURNAROUND TEST - sent by the service program to the primary to test the validity of the byte interface.

Sending a command to the SDC master is almost identical to sending data except that:

- commands should be sent to PC_CMD_WR (port 0202H) instead of PC_DATA_WR
- commands should be read from SDC_CMD_RD (location 03FE1H) instead of SDC_DATA_RD
- the action of sending a command sets the PC_CMD\DATA flag as well as the PC_BUFFER_FULL flag.

Sending a command generates the same interrupt (PC_BUFFER_FULL) as sending a data byte, and similarly, reading a command also generates the same interrupt (PC_BUFFER_EMPTY) as reading a data byte.

Commands From The SDC Master To The Host PC

Sending a command to the host PC is almost identical to sending data except that:

- commands should be sent to SDC_CMD_WR (location 03FE1H) instead of SDC_DATA_WR
- commands should be read from PC_CMD_RD (port 0202H) instead of PC_DATA_RD
- the action of sending a command sets the SDC_CMD\DATA flag as well as the SDC_BUFFER_FULL flag.

Sending a command generates the same interrupt (SDC_BUFFER_FULL) as sending a data byte, and similarly, reading a command also generates the same interrupt (SDC_BUFFER_EMPTY) as reading a data byte.

Error Status Transfer

The SDC master has the capability of writing error statuses across the byte interface. Possible error conditions are:

- iDCX Exception Error
- PC Bus Time-out

Data written to SDC_ERROR_WR (WRITE to location 03FE2H) sets the SDC_ERROR flag and the SDC_BUFFER_FULL flag. If interrupts back to the host PC are enabled, it will also generate an SDC_BUFFER_FULL (or Receive) interrupt. When the host PC reads the Error/Level 0 status, the SDC_ERROR flag is reset - an action which can be detected by the SDC master.

After an error condition the SDC master must be reset by the host PC.

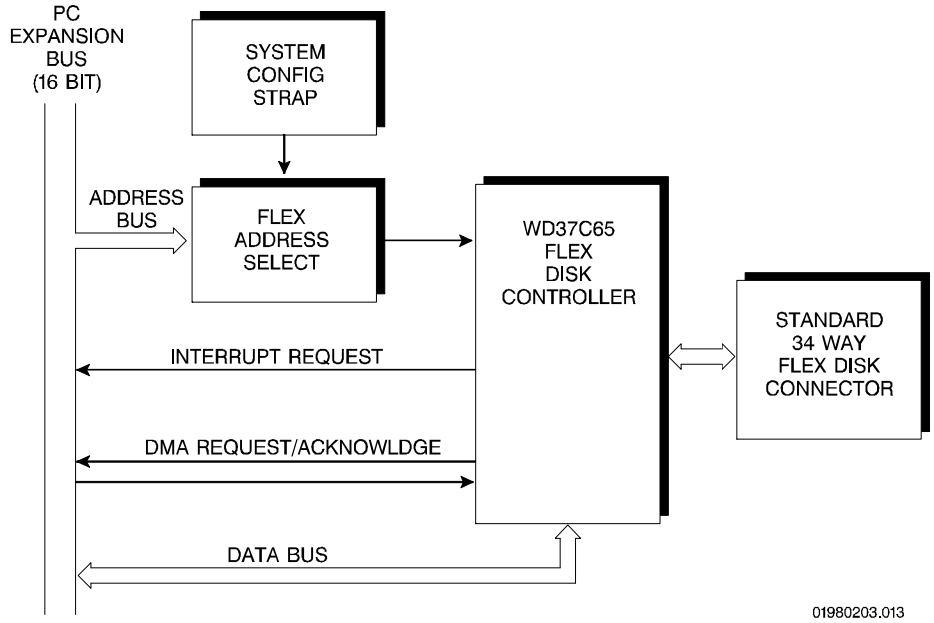
Reset of the SDC Master

The SDC master part of the SSPM can be reset from any of four possible sources:

- RESET_DRV signal from the host PC - The RESET_DRV signal is generated by the power good signal from the power supply going low. This occurs:
  - on power-up of the host PC
  - if an SDC peripheral is allowed to force the power good signal low
  - on software controlled hard reset (OUT to port 020FH). The bits 0 to 7 can have any value.
- Software reset from the host PC - The host PC can issue a reset to the SDC master by writing to port 0208H. The bits 0 - 7 can have any value.
- Power-up reset of the SDC master - An onboard circuit provides this reset signal ensuring correct start-up for board testing.
- External reset - The signal SDC_RDI_RESET is generated by an external test device to initiate level 0 diagnostics of the SDC master.

In each of the above reset conditions the reset pulse width will be greater than 15 milliseconds. Also the byte interface flags are all reset to “0” on all reset conditions.

FLEX DISK INTERFACE



The flex disk interface on the SSPM is compatible with the standard PC flex disk interface. It uses a Western Digital WD37C65 device to provide all of the functions of data rate control, pre-compensation, line driving and the writing and reading of data to and from the flex disk. It is compatible with the NCR ROM BIOS (versions 4.42 and above) and provides the interfaces for up to two flex disk drives.

The interface supports the following drives and data rates:

- 5.25 inch drives:
  - double density of 360 KBytes @ 250 Kbits per second
  - quad high density of 1.2 MBytes @ 500 Kbits per second.
- 3.5 inch drives:
  - quad density of 720 KBytes @ 250 Kbits per second
  - octal density of 1.44 MBytes @ 250/500 Kbits per second.

The SSPM flex interface can also support data rates of 125 and 300 Kbits per second and will work with dual spindle speeds of 300 or 600 r.p.m.

NCR DOS and BIOS Versions

The following are the minimum guaranteed NCR DOS and NCR BIOS versions required for the specific flex disk types supported by the SSPM:

Disk type	DOS required	BIOS required
5.25 inch (all types)	3.10 and above	4.42 and above
3.5 inch (720 KBytes)	3.20 and above	4.42 and above
3.5 inch (1.44 MBytes)	3.20 and above	4.5 and above (4.6 etc)

SSPM Flex Disk/PC Bus Interface

The host PC communicates with the flex disk controller on the SSPM via a number of I/O ports and by using DMA channel #2 and interrupt channel #6. The location of the I/O ports can be selected by Switch 20 to appear in the standard primary address at 03F0H - 03F7H or at the secondary address at 0370H - 0377H.

Switch 20	Flex Function
Off	Primary
On	Secondary

All communication with the flex disk should be done through the BIOS or through a higher means of software, but, for completeness, the actual I/O ports used are given below with the corresponding schematic signal:

Port	Read/Write	Signal	Description
03F2H/0372H	W	LDOR/	Drive Select, software reset and 0372H DMA Enable/Interrupt tri-state.
03F4H/0374H	R	CS_FLEX/	Flex controller main status register.
03F5H/0375H	W	CS_FLEX/	Command output to flex disk controller.
03F5H/0375H	R	CS_FLEX/	Flex disk controller result and status register.
03F7H/0377H	W	LDCR/	Disk data transfer speed control.
03F7H/0377H	R	READY/	Drive ready/door latch position

NOTE: A complete description of the above registers can be found in the "PC810 Technical Reference Manual".

The flex disk controller shares some I/O ports with a fixed disk controller, specifically port 03F7H/0377H, of which the flex controller only uses bit 7. For this reason, in a system which uses two flex disk controllers, one acting as a primary and the other as a secondary, if one board has a combined flex/fixed controller then it must act as the primary to permit the fixed disk controller to work with the BIOS. Before a flex controller can be used as a secondary station a device driver is required.

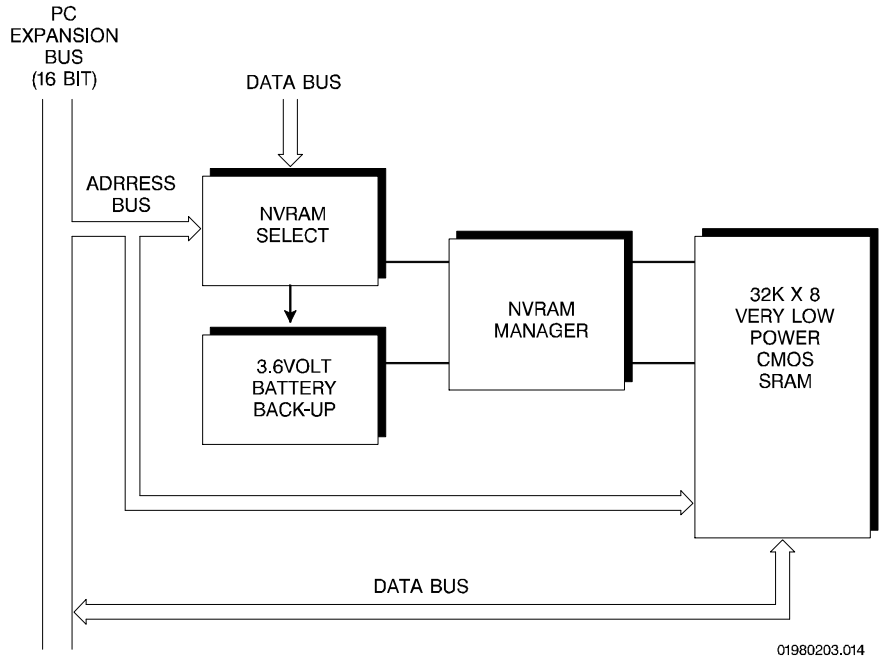
The flex disk controller on the SSPM is reset on power-up and it can also be reset from software for BIOS compatibility.

Flex Disk Only System

The SSPM can be configured to run as a flex disk only system using switches 19 and 20. When switch 19 is on and switch 20 is off the SSPM is enabled to emulate register 01F7H and allow the NCR ROM BIOS to configure the system without a hard disk.

FIXED Switch 19	FLEX Switch 20	System Configuration
Off	Off	Primary Flex/Fixed System - Default
On	Off	Primary Flex only System
Don't care	On	Secondary Flex/Fixed System

SYSTEM/SECURITY NON-VOLATILE RAM



The SSPM provides a block of 32 KBytes of battery-backed RAM acting as System and Security Non-volatile RAM (NVRAM). (This is separate from NVRAM on the SDC master). The NVRAM is accessed from the PC Bus and appears in the PC's memory space in selectable areas from 0D0000H - 0DFFFFH.

This area of memory has been designated as expansion ROM space, thus, on power-up, the PC BIOS looks for the signature of an Expansion ROM (the word identifier 0AA55H) at the first two bytes on every 2K boundary from 0C8000H - 0EFFFFH. If it finds the signature it assumes there is valid code at the address offset 3 from the 2K boundary and executes a far call to it. This condition may possibly occur in the NVRAM and so on power-up, a flip-flop is set which prevents access to the NVRAM until the address and size of the NVRAM has been setup, that is a write to I/O port 020DH (PC_NVRAM_SET).

Control of the both NVRAM sections and switching between the system +5V and the battery backup voltage is done by a Maxim 691-CPE Voltage Supervisor Controller (see sheet 2 of the schematic diagram) which controls both the supply voltage of the SRAM and its chip select. This device will switch the SRAM supply output to either the +5V supply or the battery voltage whichever is the greatest. Since there are 2 devices on the SSPM which require to be battery backed-up, the chip select input to the Voltage Supervisor is always enabled, and its output is the chip select to both of the SRAMs to be battery backed-up. If the +5V supply falls to below 4.75V the device will force the chip select high preventing data corruption and keep it to within 0.2V of the supply to the SRAM. This puts the SRAM into standby mode and reduces current consumption. The Maxim 691 itself only requires 1.0 µA in battery backup mode. Since the chip select output goes to both of the SRAMs, their write and read signals must be a function of their specific chip select and the read/write.

The area of memory that the System/Security NVRAM can be mapped into in the PC's memory map is controlled from the host PC from I/O port 020DH. System/Security NVRAM may also be disabled for benchtesting so that another card which uses the same memory space, for example an OPENNET card, may be used in conjunction with the SSPM without any contention.

Port Name	Port	Read/Write	Purpose
PC_NVRAM_SET	020DH	W	Set up system NVRAM Address and Size.

Data Bit	Function
0	NVRAM_Select_1/
1	NVRAM_Select_2/
2	Security_Select
3	}
4	}
5	} Reserved - Reset to “0”
6	}
7	}

System NVRAM

24K of NVRAM is reserved for system use, such as tallies and state-of-health information. The following codes set up the system NVRAM:

DB2	DB1	DB0	NVRAM Address
0	0	0	0D0000H - 0D5FFFH (Default)
0	0	1	0D4000H - 0D9FFFH
0	1	0	0D8000H - 0DDFFFH
0	1	1	NVRAM disabled

Security NVRAM

8 K of NVRAM is reserved for security use, although only the top 2 K is usually used.

When accessing security NVRAM it is impossible to corrupt system NVRAM and vice-versa. After access of security NVRAM, the entire block of NVRAM should either be disabled or set up as system NVRAM so that possible access and corruption following a system crash is extremely unlikely. The following codes set up the security NVRAM:

DB2	DB1	DB0	NVRAM Address
1	0	0	0D6000H - 0D7FFFH (Default)
1	0	1	0DA000H - 0DBFFFH
1	1	0	0DE000H - 0DFFFFH
1	1	1	NVRAM disabled

Data Retention

Data retention time is dependent on the duty cycle of the terminal, the power consumption of the SRAM in standby mode, and the battery capacity.

- Standby current in the range 0^{o}C to 50^{o}C:
  - 0.4 µAmp Typical
  - 5 µAmp Maximum
- Battery capacity is 1.0 Amp Hours
- Standby current of the NVRAM controller is 1 µAmp Maximum
- Data Retention for two SRAMs being battery backed-up is:
  - 90910 Hours Minimum (approx. 10.4 years)
  - 555556 Hours Typical (approx. 63 years)

The value for the maximum data retention time by far exceeds the normal shelf life of the battery which is approximately 10 years.

Transit and storage time will reduce the data retention time.

PC LEVEL 0 DIAGNOSTICS INTERFACE

The SSPM provides a set of LEDs and switches to allow level 0 execution and display of both standard and extended PC level 0 diagnostics.

Standard PC level 0 diagnostics normally report via the primary CRT Monitor on power-up of the unit, but progress reports are sent to port 0080H. The SSPM provides decoding to allow these codes to be displayed on LEDs 1-8. See Chapter 2.2 “Processor and Coprocessor, Service Aids, Testpoint Code Numbers” for a full description of these progress codes. The same LEDs are also used for extended level 0 diagnostics and display error codes sent to port 020CH in the bus interface I/O space.

Port	Read/Write	Function
0080H	W	ROM BIOS Diagnostics display
020CH	W	Extended Level 0 Diagnostics display.

In both cases the bits are assigned as follows:

Data Bit	Function	
0	LED 1	}
1	LED 2	}
2	LED 3	}
3	LED 4	} 0 tuns LED off
4	LED 5	} 1 turns LED on
5	LED 6	}
6	LED 7	}
7	LED 8	}

To distinguish between standard and extended level 0 diagnostics a separate LED is used, LED 9. If LED 9 is on, the pattern on LEDs 1-8 is a ROM BIOS generated diagnostic code. If it is off, the pattern is an extended level 0 diagnostic code.

The execution of a particular extended level 0 test may be defined using switches 1-7:

Port	Read/Write	Function
020CH	R	Extended Level 0 test input.

The bits are assigned as follows:

Data Bit	Function	
0	Switch 1	}
1	Switch 2	} Switch Open - Logic “0”
2	Switch 3	} Switch Closed - Logic “1”
3	Switch 4	}
4	Switch 5	}
5	Switch 6	}
6	Switch 7	}
7	Supervisor Switch Input	

NOTE: The selection of PC level 0 tests using the switches is a future option and is not in place on the current SSPMs, however switch SW1 has the function of clearing system NVRAM when the terminal is reset or powered on. Refer to the “Strapping” section of this chapter and to Chapter 2.2 in the section “Extended ROM BIOS Diagnostics” for more information on this switch.

SUPERVISOR SWITCH

Bit 7 of I/O port 020CH reports the state of the Terminal Supervisor Switch (if implemented). It is connected to J10, a 3-way right-angle connector. The state of the bit is defined as follows:

- Logic “0” - Supervisor Switch Open - Terminal in Supervisor Mode
- Logic “1” - Supervisor Switch Closed - Terminal in Normal Mode.

SOFTWARE CONTROLLED HARDWARE RESET

The host PC may reset the entire PC Core by writing to I/O port 020FH. The bits 0-7 can have any value.

A monostable lengthens the resultant pulse to a minimum of 100 ms and this then drives an open collector gate to force the power-good signal of the PC power supply low. This is picked up by the main processor board which then drives RESET_DRV on the PC Bus Board active high, resetting all the hardware in the PC Core. To avoid any possible contention, the software controlled hard reset is only allowed when the RESET_DRV signal is inactive and the active low strobe for the monostable is pulled high via a pull-up resistor.

GRAPHICS ADAPTER

The SSPM has a 62-way connector and mounting holes for use with NCR EGA and VGA piggy-back modules. The signals on this interface are taken directly from the PC Bus.

NOTE: If the EGA piggy-back option is used, the SSPM requires the space of 2 adjacent 0.8 in. slots on the PC motherboard/busboard or a single 1.0 in. slot.

MEMORY EXPANSION

The SSPM has a 62-way connector and mounting holes for use with NCR 1 MByte and 4 MByte memory expansion piggy-back modules. The signals for this interface are taken directly from the PC Bus.

NOTE: If the memory expansion piggy-back option is used, the SSPM requires the space of 2 adjacent 0.8 in. slots on the PC motherboard/ busboard or a single 1.0 in. slot.

ADDRESS AND INTERRUPT LINE SELECTION

Switches 17 and 18 on the SSPM are provided to allow the user to select 1 of 4 possible locations of the PC - SDC master bus interface in the PC's I/O space (see table in the section “PC Bus Interface”.

One switch (S20) is provided to allow the user to select between primary or secondary addresses for the SSPM's flex disk controller.

The software must also be configured so that it reads/writes from the correct area of I/O space and also sets up an interrupt routine for the correct interrupt vector.

SDC LINK

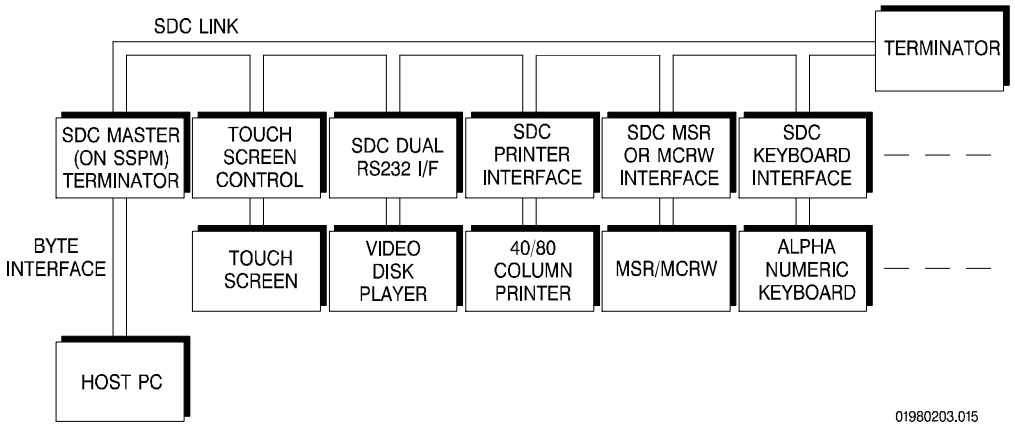
The hardware components of the SDC link are:

- Master node
- Slave node interfaces
- Repeater node
- Interconnect cabling.

The software and firmware components are:

- SDC Service software
- SDC Primary Firmware
- SDC Secondary Peripherals software.

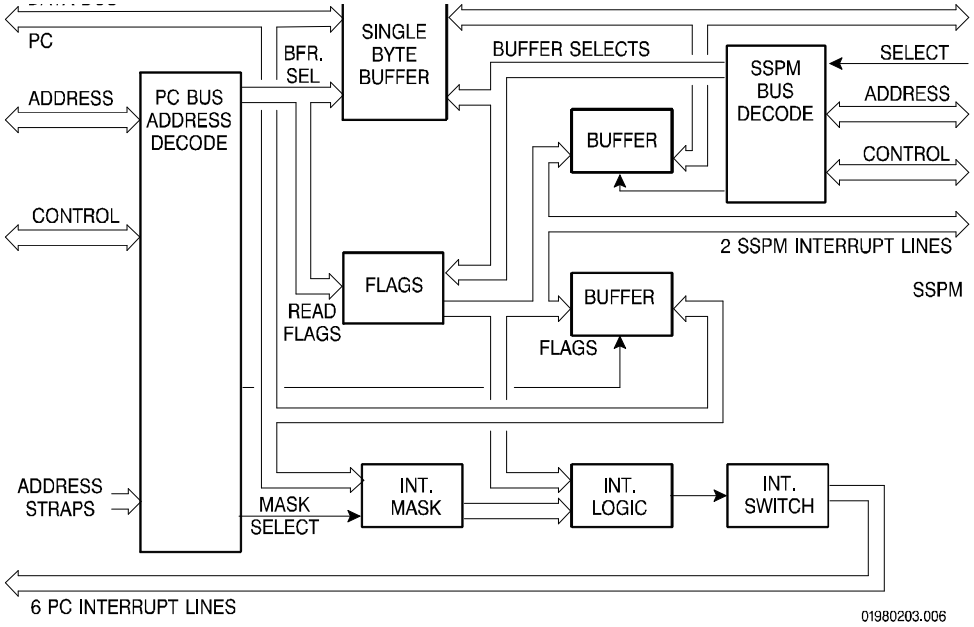
The block diagram following shows the implementation of the SDC link in the 5682 Self Service Terminal.



MASTER NODE

The master node is described in the section “Self Service Personality Module - SDC Master”.

SLAVE NODE INTERFACES



This section should be read in conjunction with the Schematic Diagram for the SDC Secondary Node - see page FO - 17.

The link interface hardware is based on an INTEL 8032 processor (or equivalent) operating at 12MHz. This processor performs the link interface functions and the device control functions.

The link interface uses the 8032 serial communications port operating in mode 2, the physical link interface connection is via RS485 transceivers.

The 8032 memory is implemented as external EPROM and external SRAM. The EPROM generally contains level 0 diagnostics and the link interface firmware and the SRAM normally contains the downloaded device firmware and data areas. However, there will be exceptions to this, such as the basic encryptor.

Non-volatile storage for state-of-health requirements is implemented by battery-backing the SRAM and reserving the appropriate area as NVRAM.

An SDC level 0 diagnostic interface is implemented using 4 LED indicators on 8032 ports P1.0-P1.3, and 8 switches at memory mapped I/O port 3FF8H.

A 512 byte area in the Data Area (3E00H-3FFFH SDC1, 1E00-1FFFH SDC2) is reserved for memory mapped I/O ports. I/O port 3FF8H (SDC1), 1FF8H (SDC2) is reserved for Level 0 diagnostic use, the remainder are used for device control.

A Field Programmable Logic Array (FPLA) performs memory mapping, data transceiver control, and provides a number of device selects and/or Read/ Write strobes and, optionally, a test input for manufacturing test.

Processor

The processor is an 8032 device operating at a clock rate of 12MHz. The 8032 internal oscillator and an external crystal provide the clock source, although an external oscillator may be used. The 12MHz frequency is the maximum for an 8032 and provides a sufficiently high transfer rate on the SDC link (187.5 Kbits/sec) with the onboard UART operating in mode 2. (Clock Frequency/64).

The processor's integrated I/O ports are assigned as follows:

Port	Function	
P0.0-P0.7	Multiplexed Address/Data Bus : AD0-7	
P2.0-P2.7	High Address Bus : A8-15	
P1.0	LED Indicator 1	}
P1.1	LED Indicator 2	} 0 - OFF, 1 - ON
P1.2	LED Indicator 3	}
P1.3	LED Indicator 4	}
P1.7	Transceiver Control 0- Transmit, 1 - Receive	
P3.0	SDC Receive Data : RXD	
P3.1	SDC Transmit Data : TXD	
P3.6	Data Memory Write Strobe : WR/	
P3.7	Data Memory Read Strobe : RD/	
	All other ports are unassigned.	

The address/data bus is demultiplexed using a 74LS373 octal transparent latch strobed by ALE. This device is located next to the 8032 to minimize noise and grounding problems.

Bus loading requires that the data bus (AD0-7) is buffered using a 74LS245 octal transceiver. The transceiver is always enabled to allow data through. Direction is controlled by 8032_READ/ which is generated by the FPLA during both Code and Data bus cycles. The transceiver is located close to the 8032.

The 8032 External Access pin (31) is grounded to force all memory access to be external.

Memory

The 8032 operates with two independent external memory areas; a Code Area containing the program code and a Data Area containing data. The two memory areas share the same address and data buses but are accessed via different control signals. The 8032 expects the Code Area to be Read Only and so generates Program Store Enable (PSEN/) to act as an output enable control for an EPROM. The Data Area must be read/write therefore the 8032 generates RD/ and WR/ to access SRAM.

Memory Map Requirements

To facilitate the download of device control code, the read/write memory which contains this code must appear in the Data Area during download and in the Code Area during execution.

The 8032 executes from address 0000H after reset, therefore, the lower portion of the Code Area must be populated with EPROM containing start-up code.

A further constraint on the memory map is imposed by the iDCX-51 executive which requires a 256 byte data area located at 0000H-00FFH.

The 8032 does not directly support external I/O ports, therefore part of the Data Area must be allocated as memory mapped I/O ports.

Memory Map Implementation

This section describes the memory map implementations which meet the above constraints.

Minimum Hardware Implementation

The minimum hardware implementation which meets the requirements is as follows:

The lower 8 K, 16 K or 32 KBytes of Code Area is populated with a single EPROM device, the size required being dependent upon the application.

The Data Area is populated as follows for one 32 K x 8 SRAM:

- SRAM from 8200H - 0FFFFH.
- The upper 32K bytes (minus 512 bytes) of Code Area is mapped into the corresponding Data Area to facilitate download and execution of code and also data storage
- The physical bottom 512 bytes of the populated Data Area (8000H - 81FFH) is mapped to appear at logical address 0000H-01FFH in the Data Area.
- The conditions above provide a 512 byte data area for iDCX-51 and SDC firmware without the need to physically locate additional SRAM at the bottom of the Data Area. The resulting 512 byte “hole” at 8000H-81FFH in both Code and Data Areas is unusable.

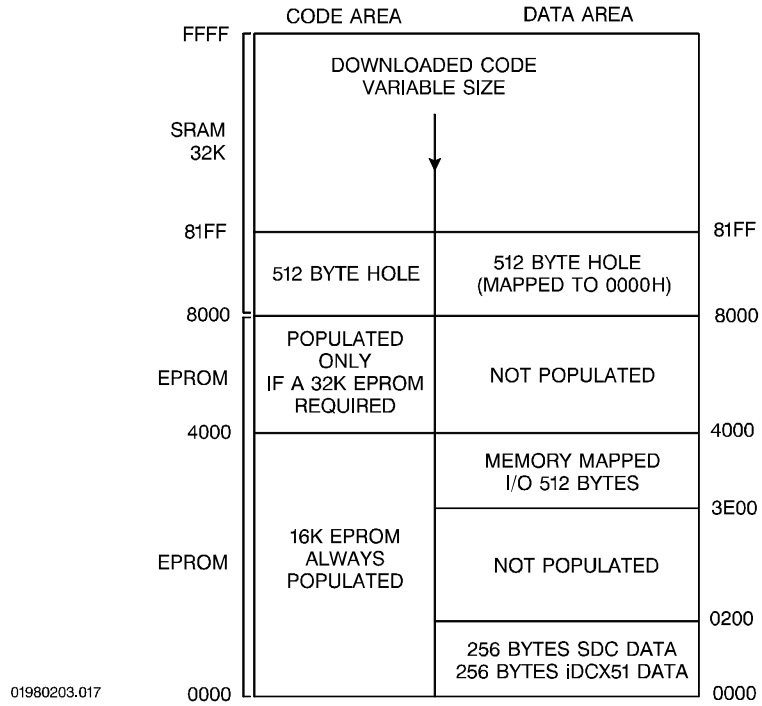
The Data Area is populated as follows for two 32 K x 8 SRAMs:

- SRAM from 0000H - 0FFFFH.
- The upper 32 K, 48 K, or 56 KBytes of Code Area is mapped into the corresponding Data Area to provide either 32 K, 48 K, or 56 KBytes of downloadable code area dependent upon the EPROM size.

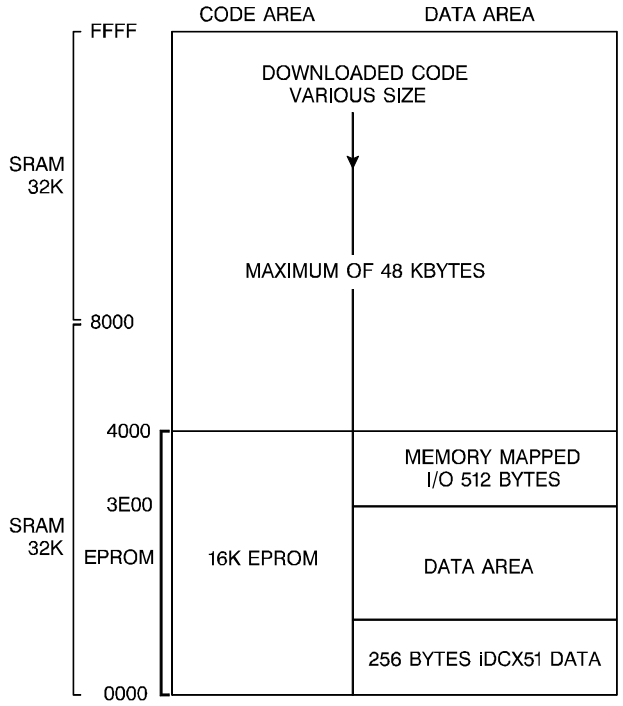
For both implementations, a 512 byte area in the Data Area is allocated as memory mapped I/O ports. SDC1 nodes (minimum 16 KBytes EPROM) use 3E00H-3FFFH and SDC2 nodes (minimum 8 KBytes EPROM) use 1E00H-1FFFH as I/O space. Since this always corresponds to an EPROM address in the Code Area, it provides I/O expansion without impacting the shared downloadable code/data area. This area in the data space is unusable for data storage.

8032 Memory Map

SDC1 (16 K or 32 KBytes EPROM, 32 KBytes SRAM)

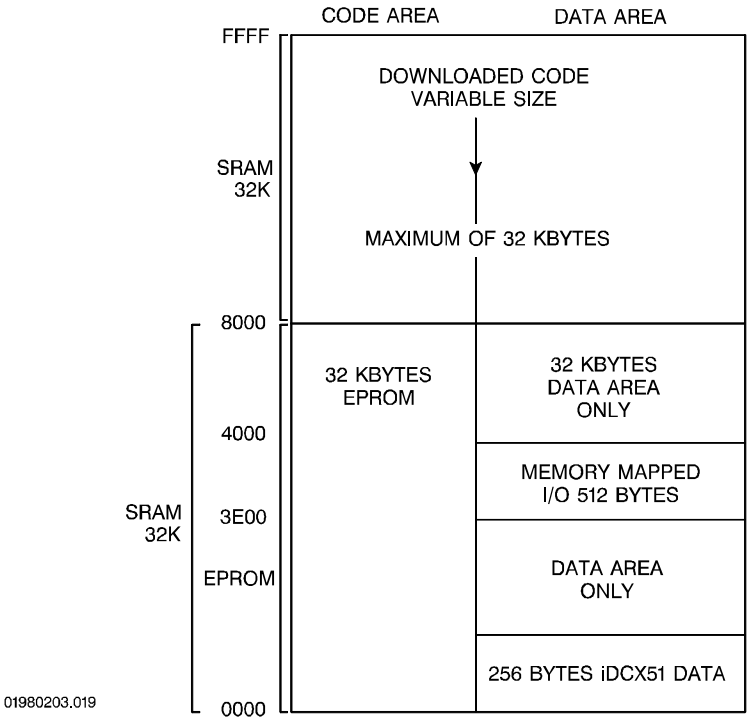


SDC1 (16 KBytes EPROM, 64 KBytes SRAM)

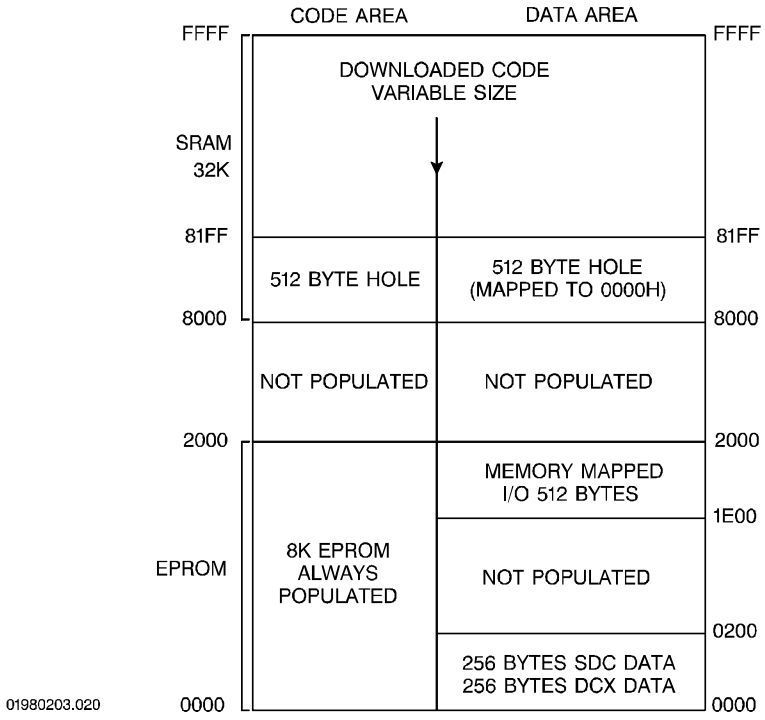


01980203.018

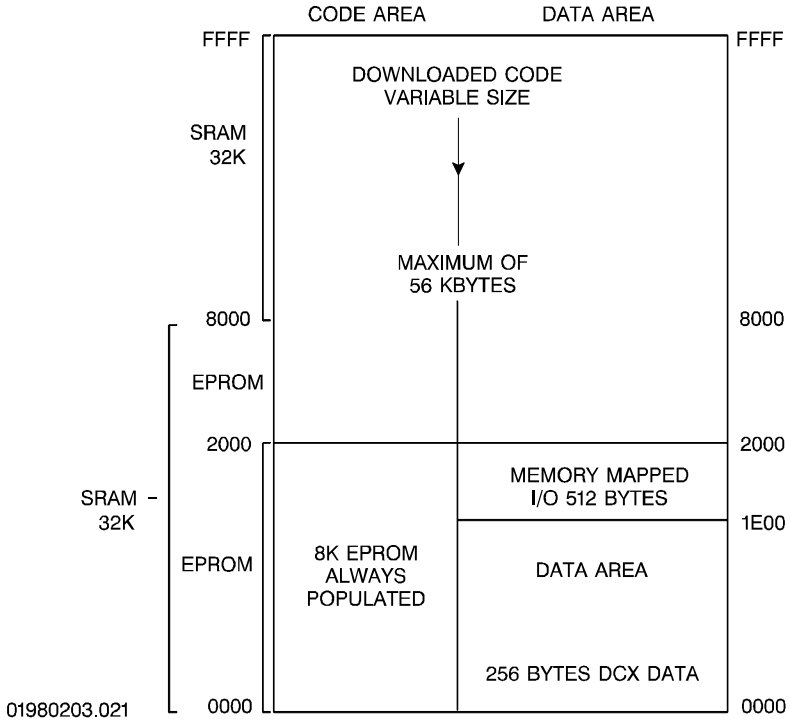
SDC1 (32 KBytes EPROM, 64 KBytes SRAM)



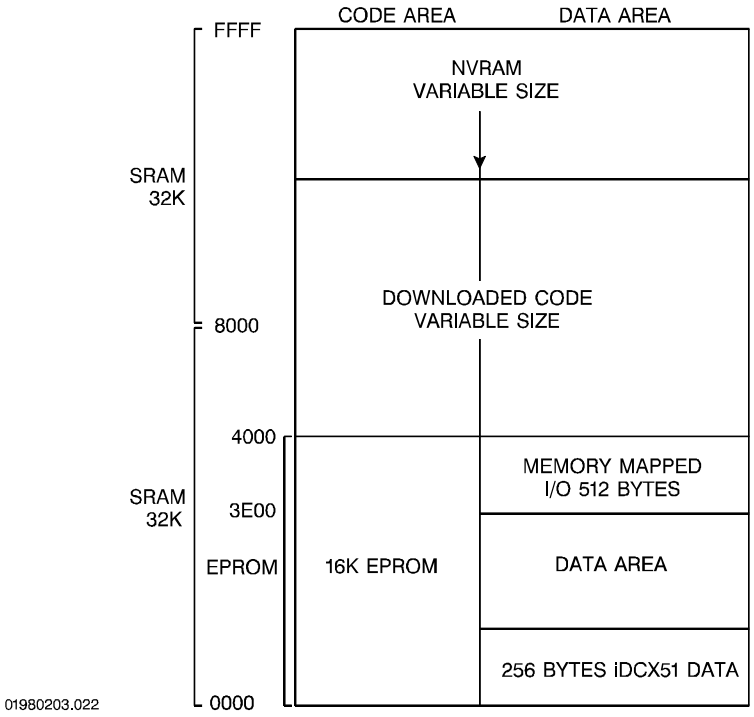
SDC2 (8 KBytes EPROM, 32 KBytes SRAM)



SDC2 (8 KBytes EPROM, 64 KBytes SRAM)



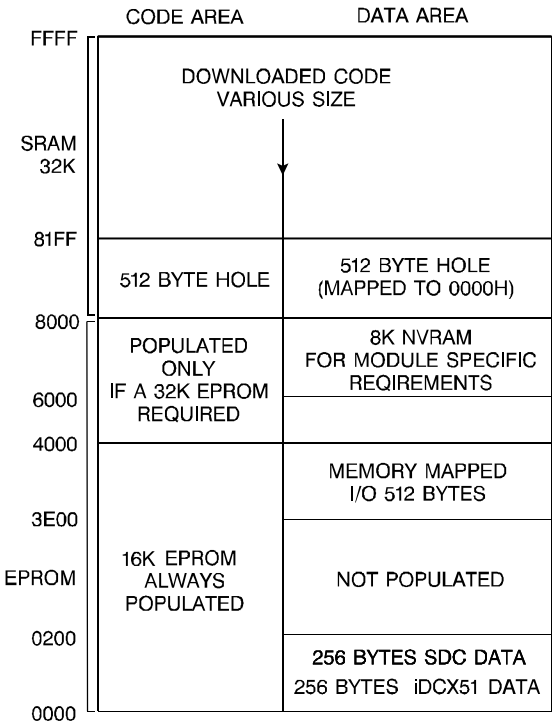
SDC1 (16 KBytes EPROM 64 KBytes SRAM With Example NVRAM)



Optional NVRAM for State-Of-Health requirements is implemented as battery backed-up SRAM located from the top of data memory downwards. A small section of a battery-backed 32K SRAM is used for NVRAM. The amount used is specified as a base address at the top of NVRAM so that level 0 diagnostics will not overwrite the NVRAM on reset.

NVRAM is also mapped into the code space and so may be used to backup the downloaded device-driver. To accommodate this, there is onboard tracking for a second battery-backed SRAM. (Refer to the schematic for details).

SDC1 (16 K or 32 KBytes EPROM 32 KBytes SRAM, 8 K NVRAM)



01980203.023

Any separate NVRAM requirements, say for Key Storage on SDC Encryptor nodes, will use either a separate 8K or 32K battery backed SRAM located from memory address 7FFFH downwards.

Control Signal Decoding

A PLS173 FPLA provides the necessary control signals to implement the memory map. The control signals are decoded as follows:

SDC1 (16 KBytes EPROM, 32 KBytes SRAM)

8032_READ/	= {PSEN + RD}/	
EPROM Select/	= CSROM/	
	= {A15/.A14/.TEST_INPUT}/	Only if TEST_INPUT is put in the FPLA.
EPROM		
Output Enable/	= PSEN/	
SRAM Select/	= CSRAM/	
	= {A15.A14	)
	+ A15.A13	) 81FF-FFFF
	+ A15.A12	)
	+ A15.A11	) Code or Data
	+A15.A10	)
	+ A15.A9	)
	+ A15/.A14./A13/.A12/.A11/.A10/	) 0000-01FF
	.A9/.WR.	) Data Only
	+A15/.A14/.A13/.A12/.A11/.A10/.A9/ .RD/}/	)

SDC1 (32 KBytes EPROM, 32 KBytes SRAM)

8032_READ/	= {PSEN + RD}/	
EPROM Select/	= CSROM/	
	= {A15/.TEST_INPUT}/	Only if TEST_INPUT is put in the FPLA.
EPROM		
Output Enable/	= PSEN/	
SRAM Select/	= CSRAM/	
	= {A15/.A14	)
	+ A15.A13	) 81FF-FFFF
	+ A15.A12	)
	+ A15.A11	) Code or Data
	+ A15.A10	)
	+ A15.A9	)
	+ A15/.A14/.A13/.A12/.A11/.A10/.A9/ .WR	) 0000-01FF
	+ A15/.A14/.A13/.A12/.A11/.A10/.A9/ .RD/}/	) Data Only

SDC1 (16 KBytes EPROM, 64 KBytes SRAM)

8032_READ/	= {PSEN + RD}/	
EPROM Select/	= CSROM/	
	= {A15/.A14/.TEST_INPUT}/	Only if TEST_INPUT is put in the FPLA.
EPROM		
Output Enable/	= PSEN	
SRAM1 Select/	= CSRAM1/ {A15}/	8000-FFFF Code or Data
SRAM2 Select/	= CSRAM2/	
	= {A15/.A14	4000-7FFF Code or Data
	+ A15/.A14/.A13/.WR	)
	+ A15/.A14/.A13/.RD	)
	+ A15/.A14/.A12/.WR	)
	+ A15/.A14/.A12/.RD	) 0000-3E00 Data
	+ A15/.A14/.A11/.WR	) Only
	+ A15/.A14/.A11/.RD	) Omits Memory
	+ A15/.A14/.A11/.WR	) Mapped I/O
	+ A15/.A14/.A10/.RD	)
	+ A15/.A14/.A9/.WR	)
	+ A15/.A14/.A9/.RD}/	)

SDC1 (32 KBytes EPROM, 64 KBytes SRAM)

8032_READ/	= {PSEN + RD}/	
EPROM Select/	= CSROM/	
	= {A15/.TEST_INPUT}/	
EPROM		
Output Enable/	= PSEN	
SRAM1 Select/	= CSRAM1/ {A15}/	8000-FFFF Code or Data
SRAM2 Select/	= CSRAM2/	
	= {A15/.A14.WR	) 4000-7FFF
	+ A15/.A14/.RD	) Code or Data
	+ A15/.A14/.A13/.WR	)
	+ A15/.A14/.A13/.RD	)
	+ A15/.A14/.A12/.WR	)
	+ A15/.A14/.A12/.RD	) 0000-3E00
	+ A15/.A14/.A11/.WR	) Data Only
	+ A15/.A14/.A11/.RD	) Omits Memory
	+ A15/.A14/.A10/.WR	) Mapped I/O
	+ A15/.A14/.A10/.RD	)
	+ A15/.A14/.A19/.WR	)
	+ A15/.A14/.A9/.RD}/	)

SDC2 (8 KBytes EPROM, 32 KBytes SRAM)

8032_READ	= {PSEN + RD}/	
EPROM Select/	= CSROM/	
	= {A15/.A14/.A13/.TEST_INPUT}/	Only if TEST_INPUT is put in the FLPA
EPROM		
Output Enable/	= PSEN/	
SRAM Select/	= CSRAM/	
	= {A15.A14	)
	+ A15.A13	) 81FF-FFFF
	+ A15.A12	)
	+ A15.A11	) Code or Data
	+ A15.A10	)
	+ A15.A9	)
	+ A15/.A14/.A13/.A12/.A11/.A10/.A9/.WR	) 0000-01FF
	+ A15/.A14/.A13/.A12/.A11/.A10/.A9/.RD/}/	) Data Only

SDC2 (8 KBytes EPROM, 64 KBytes SRAM)

8032_READ/	= {PSEN + RD}/	
EPROM Select/	= CSROM	
	= {A15/.A14/.A13/.TEST_INPUT}/	Only if TEST_INPUT is put on the FPLA
EPROM		
Output Enable/	= PSEN/	
SRAM1 Select/	= CSRAM1/ {A15}/	8000-FFFF Code or Data
SRAM2 Select/	= CSRAM2/	
	= {A15/.A14	4000-7FFF Code or Data
	+ A15/.A14/.A13	2000-3FFF Code or Data
	+ A15/.A14/.A13/.A12/.WR	)
	+ A15/.A14/.A13/.A12/.RD	)
	+ A15/.A14/.A13/.A11/.WR	)
	+ A15/.A14/.A13/.A11/.RD	) 0000-1E00
	+ A15/.A14/.A13/.A10/.WR	) Data Only
	+ A15/.A14/.A13/.A10/.RD	) Omits Memory
	+ A15/.A14/.A13/.A9/.WR	) Mapped I/O
	+ A15/.A14/.A13/.A9/.RD	)

NOTE: All EPROMs have access times of 200ns or less and all SRAMs have access times of 120ns or less.

I/O Expansion

When used with external memory, most of the 8032 integrated I/O port pins are dedicated as address, data and control lines. I/O ports must therefore be created on the 8032 bus. Since the 8032 does not directly support external ports, expansion ports must be memory mapped I/O. The SDC secondary interface has a 512 byte area of the Data Area (3E00H-3FFFH) allocated for this purpose. The resulting “hole” in the Data Area is unusable for memory storage.

The memory mapped I/O area for SDC1 nodes is 3E00-3FFFH and for SDC2 nodes is 1E00-1FFFH.

Address lines A9-A15 are decoded to select the I/O block. Address lines A3-A5 are decoded to select groups of eight I/O ports within the I/O block.

I/O Select Lines

The same FPLA which generates the memory select lines is used to generate the I/O select lines. Pin availability on the device limits the number of selects to six. By including the 8032 Read and Write strobes in the decode equations, the FPLA outputs can be device selects and/or I/O read/write strobes. Since each select line is active for a group of eight port addresses, the select line can be further decoded external to the FPLA with the lower addresses, A0-A2, to produce additional selects if required.

The I/O select signals are decoded as follows for SDC1:

- CONFIG_RD/ = (READ 3FF8H-F) - This is always required = {A15/.A14/.A13.A12.A11.A10.A9.A5.A4.A3.RD}/
- CS3FF0-7/ = {A15/.A14/.A13.A12.A11.A10.A9.A5.A4.A3/}/
- CS3FE8-F/ = {A15/.A14/.A13.A12.A11.A10.A9.A5.A4/.A3}/
- CS3FE0-7/ = {A15/.A14/.A13.A12.A11.A10.A9.A5.A4/.A3/}/
- CS3FD8-F/ = {A15/.A14/.A13.A12.A11.A10.A9.A5/.A4.A3}/
- CS3FD0-7/ = {A15/.A14/.A13.A12.A11.A10.A9.A5/.A4.A3/}/

The I/O select signals are decoded as follows for SDC2:

- CONFIG_RD/ = (READ 1FF8H-F) - This is always required {A15/.A14/.A13/.A12.A11.A10.A9.A5.A4.A3.RD}/
- CS1FF0-7/ = {A15/.A14/.A13/.A12.A11.A10.A9.A5.A4.A3/}/
- CS1FE8-F/ = {A15/.A14/.A13/.A12.A11.A10.A9.A5.A4/.A3}/
- CS1FE0-7/ = {A15/.A14/.A13/.A12.A11.A10.A9.A5.A4/.A3/}/
- CS1FD8-F/ = {A15/.A14/.A13/.A12.A11.A10.A9.A5/.A4.A3}/
- CS1FD0-7/ = {A15/.A14/.A13/.A12.A11.A10.A9.A5/.A4.A3/}/

NOTE: 1. If two 32 KByte SRAMs are used the number of available selects is decreased by one.

NOTE: 2. One of the FPLA bidirectional lines can be used as an input for manufacturing test to disable the onboard EPROM, however this may also be accomplished by using a spare gate.

NOTE: 3. Since address lines A8-A6 are not used in the decoding, only I/O ports in the range 3FC0H - 3FFFH (SDC1) and 1FC0H-1FFFH (SDC2) are valid if extra decoding is required.

NOTE: 4. If required, the above I/O selects may be either read or write strobes or may be simply address strobes with the read and write signals being additional qualifiers on the particular I/O device. This may be necessary for timing requirements.

Level 0 Diagnostic Interface

The SDC secondary interface includes EPROM based level 0 diagnostics which execute after reset or power-up and test the functions of the SDC link interface hardware. The diagnostics test the Processor, EPROM, SRAM and also provide selectable transmit and receive tests on the SDC link but do not test any functions specific to the peripheral. Diagnostic test results are displayed on LED indicators. Test modes are controlled via on board switches. Access to the indicator and switch signals is available on a connector to facilitate control of the diagnostics from an external piece of test equipment. The SDC secondary node can also be reset from the external test device.

Diagnostic Indicators

Diagnostic test results are displayed on a group of four LED indicators (LEDs 1 to 4). These indicators are connected to the 8032 ports P1.0-P1.3 via inverting drivers. Outputting a “1” to the port pin turns the LED on, a “0” turns it off. Since Reset sets all 8032 port pins to “1”, the LEDs are on after Reset until switched off by the diagnostics.

Diagnostic Switches

Diagnostic test execution is controlled via a group of eight switches (SW1 to SW8). These switches are read by the 8032 at memory mapped I/O port 3FF8H (SDC1) or 1FF8H (SDC2). Connection to the 8032 data bus is through inverting drivers, therefore, a CLOSED switch returns a “1” on the data bus and an OPEN switch a “0”. Switches SW1-SW8 correspond to data bits 0-7 respectively.

SDC Secondary Node Reset Conditions

The SDC secondary node is reset on the following conditions:

- Power-Up and Power-Down - The 8032 will be held reset for at least 50 ms after the +5 V signal rises above 4.7V. Also if the +5 V drops below 4.6 V, the 8032 will be reset
- SDC Reset - The SDC secondary node will be reset by a node driving the differential SDC reset lines active. The length of this reset pulse is at least 200 ms.
- External Diagnostics Reset - This is a reset from an external test device. It should be at least 50 ms in length.

SDC LINK INTERFACE

The SDC link is a multipoint link which uses the EIA RS485 standard for its electrical interface. This standard defines a bidirectional, multipoint connection using differential transmitters and receivers.

The SDC link comprises four circuits, DATA, RESET, TRANSCEIVER ENABLE, and SIGNAL REFERENCE. DATA and RESET is implemented by all SDC secondary devices. TRANSCEIVER ENABLE and SIGNAL REFERENCE are optional and need only be implemented by secondary devices which will connect to repeater segments of the link.

The three RS485 signals, DATA, RESET, and TRANSCEIVER ENABLE, are differential signals carried on pairs of wires. The signal pairs are identified by "+" and "-", for example DATA+ and DATA-. The signal is active or in a logical "1" state when DATA+ is more positive than DATA-.

The electrical interface to the link is via 75176 Transceiver circuits.

DATA

The DATA signal is a bidirectional signal. The receive data signal, RXD, is connected to the 8032 serial port receive pin, P3.0. The transmit data signal, TXD, is connected to the 8032 serial port transmit pin, P3.1. The receive enable pin on the transceiver is grounded, thus permanently enabling the receiver. Reception of data is enabled/disabled under software control within the 8032. The transmit enable pin is controlled by 8032 port P1.7. This signal is passed through an inverter to make sure that the transmitter is disabled after Reset. Because transmitted data is also fed back to the receive pin, interrupts from the receive are disabled before transmission.

RESET

The RESET signal is a bidirectional signal. It is generated by the master node and received by all secondary nodes. A secondary node will not normally generate RESET, the exception being an operator panel which includes a System Reset switch. In this case all nodes, including the master node, will receive the RESET signal. On nodes which do not generate RESET, the transceiver will be permanently held in the receive state with its transmitter disabled.

A device which generates RESET cannot reside on a repeater segment of the link, it must reside on the master segment.

RESET is active when RESET+ is more positive than RESET-. When active it will reset the 8032. RESET is normally biased by either an SDC master node or a repeater node to be inactive unless driven active high.

After a reset condition on the SDC master node, a 260 millisecond RESET pulse on the SDC link will be issued.

TRANSCEIVER ENABLE

The TRANSCEIVER ENABLE signal is required to control the direction of the transceivers in a repeater node. Devices which will not be located outside the host unit need not implement this circuit. It is activated by a secondary node when that node is transmitting data to the master node. It turns the DATA transceiver within a repeater node to point towards the master node. The signal is generated by repowering the secondary node's internal Transmit Enable through a 75176 transceiver.

SIGNAL REFERENCE

SIGNAL REFERENCE is a single signal required on a repeater segment node, to balance any current loops between SDC nodes which may have different earth potentials.

SDC Link Connector - Nodes connect to the link via 10 way (Dual 5) latch ejection headers with Male pins.

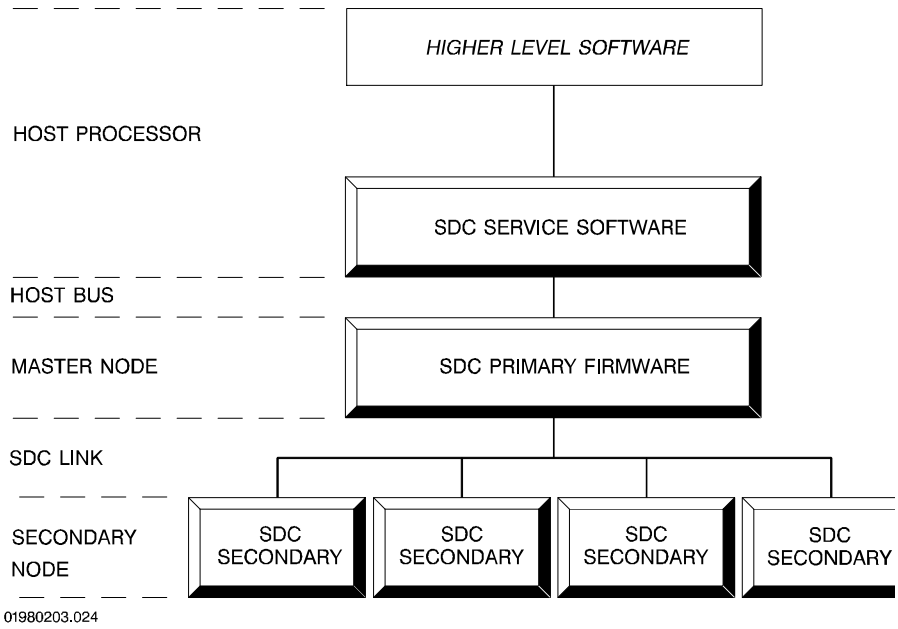
The connector may be either straight or right-angled depending on implementation. (See “Service Aids - Connector Pinouts”).

INTERCONNECT CABLING

Refer to the section “Service Aids - Cable Information” for a diagram of the SDC link cable.

SDC SOFTWARE AND FIRMWARE

The SDC Subsystem is a layered network of both firmware and software functions which are invoked to cause devices on the link to perform specific operations. The layers are illustrated in the following figure:



SDC SERVICE SOFTWARE

The SDC Service Software is PC-resident software which provides an interface between the higher level software and the SDC subsystem. It passes commands and receives responses from the SDC primary for transfer to and from SDC secondary peripherals.

SDC PRIMARY FIRMWARE

The SDC primary firmware interfaces the SDC Service Software to the SDC secondary peripherals via the SDC communications link. The SDC primary is responsible for sending commands and polling for responses from the SDC secondary peripherals. A priority based polling scheme is adopted to optimize utilization of the SDC link to achieve fast reporting of unsolicited input for secondary peripherals governed by human factors guidelines, for example, key depression detect within 25ms. Adequate slower response is provided for devices which limit transaction speed (for example within 100ms for the MCRW).

The SDC Primary firmware is divided into two parts; the Primary Manager and the Primitives. All errors on the SDC link are reported to the primary manager by the primary SDC communication primitives. The primary manager is responsible for maintaining error counts for all SDC link errors.

SDC SECONDARY PERIPHERALS SOFTWARE

The dedicated software associated with secondary peripherals is located in the hardware node PCB associated with the peripheral. The device driver may be either located in PROM or be downloaded across the SDC link from the host to RAM.

SDC LINK PROTOCOL

The SDC link protocol provides the data transfer between the primary and its addressed secondaries. It is the responsibility of the primary manager to manage the SDC link, that is, to provide error control and to achieve communications with the addressed secondary devices.

SERVICE AIDS

EQUIPMENT REQUIRED

The equipment required to service the SSPM is:

- PC Rig providing +5V, +12V, -12V
- Oscilloscope
- SDC secondary nodes to correctly test the SDC link.

The following onboard facilities are provided for fault diagnosis of the SSPM:

- Transmit and receive tests on the SDC link
- SDC level zero diagnostics to test the SDC master
- PC diagnostic switches and LEDs for extended and BIOS level zero error reporting.

VOLTAGE AND CURRENT

The SDC link interface circuits (primary and secondary nodes) require:

- +5 V $\pm$ 0.25 V.

The SSPM requires the following voltages:

- +5 V $\pm$ 0.25 V at 2 A maximum
- 3.6 V $\pm$ 0.2 V at 1.8 µA typical battery supply to static RAM
- -1.0 V at 11 µA maximum in power down state.

LEVEL 1 DIAGNOSTICS

Level 1 diagnostics tests for the flexible disk drives are described in Chapter 9.3.

PC LEVEL 0 AND EXTENDED ROM BIOS DIAGNOSTICS

The results of PC level 0 and extended ROM BIOS diagnostic tests are displayed on LEDs 1-8 on the SSPM. LEDs 9 and 14 on the SSPM define which codes are being displayed. The test codes are described in Chapter 2.2.

SDC LEVEL 0 DIAGNOSTICS

The Diagnostic Subsystem (DS) is firmware which executes automatically when a Serial Distributed Controller is powered on, or receives an on or off-board generated reset. It will execute in Start-Up mode and Test mode.

Start-up mode comprises a set of tests which execute in sequence to check the basic functions of the SDC core (8032 ALU and internal functions, EPROM and SRAM) .

Start-up does not require operator intervention, and, if it is successful, it passes control to the application firmware.

Test mode comprises a set of more comprehensive tests which may need operator intervention, for example, to put on turnaround plugs. Selected tests may be run individually, in single pass, or loop, with stop or continue-on-error options.

Control of the DS is via a bank of 8 switches and test results are displayed on a bank of 4 LEDs. The DS may also be controlled via a Remote Diagnostics Interface (RDI) connector which provides access to the switches, LED and Reset signals.

On the SDC master the DS may be controlled by PC Application (PCA) via the PC-Bus byte interface.

SWITCHES AND LEDS INTERFACE

The numbering of the switches and LEDs differs between the SSPM master node and the SDC slave nodes. On the SSPM the switches are numbered SW 9 to SW 16 and the LEDs are numbered LED 10 to LED 13 whereas on the SDC slave node boards the switches are numbered SW 1 to SW 8 and the LEDs are LED 1 to LED 4. In the following description the slave node numbering is used. **Remember to add 8 to get the equivalent switch number on the SSPM and 9 for the LED number.**

Switches

The switch settings are examined only after a system reset occurs. Any changes to the switch setting thereafter will be ignored. If an illegal test number or mode is set up on the switches the DS will ignore the settings and will display “DH” on the LEDs.

Mode Option

Switch SW8 is used to determine which method of testing is to be used. If SW8 is “OFF” then diagnostics are performed in start-up mode. If SW8 is “ON” then diagnostics are run in test mode (that is, either selected or run-to-run tests).

Loop Option

Switch SW7 is used to define the action taken on completion of a test or test sequence. If SW7 is "ON" then the test or test sequence is repeatedly executed if no error occurs.

NOTE: If SW6 is "ON" but SW7 is "OFF" then a bad switch setting error will be reported.

Continue On Error Option

Switch SW6 defines the action taken when Loop Option is selected and an error is reported during test or test sequence execution. With SW7 "ON" and also SW6 "ON" the test or test sequence will run indefinitely even if an error is reported. SW6 is only valid if SW7 is on.

Onboard Switch Settings

The onboard switch settings are as shown in the following table:

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Start-up:								
Master Node	0	0	0	0	0	0	0	0
Slave Node	X	X	X	X	X	X	X	X
Run-to-Run	0	0	0	0	0	SW6	SW7	1
Selected	<---------- TEST ID ---------->				0	SW6	SW7	1

0 = Switch OFF/OPEN
1 = Switch ON/CLOSED

SW7 - Loop Option
OFF = Run test sequence once
ON = Run test sequence indefinitely (according to error option)

SW6 - Error Option (valid only if SW7 is ON)
OFF = Halt on error
ON = Continue on error

LEDs

While a test is being executed its test number is displayed on LEDs 1-3. LED 4 "OFF".

For example:

LED	**4**	**3**	**2**	**1**
	0	<- TEST ID >		

On successfully completing a test the DS will either jump to the next test without displaying a pass code if running a test sequence, or, if running a selected test, the DS displays the test ID for one second and then the pass code for two seconds.

If a test fails the DS displays the test ID for one second and then the error code for two seconds.

NOTE: LED 4 is always “ON” if an error code is being displayed.

Examples

- Test 4 with Loop but no Error Option:

Test Number	Test Result
	LEDs
4	4 - Test executing
4	0 - Pass Code
4	4 - Test executing
4	9 - Test fails with error 9H and LEDs alternate between displaying 9H and 04H

- Test 4 with Loop and Error Option:

Test Number	Test Result
	LEDs
4	4 - Test executing
4	0 - Pass Code
4	4 - Test executing
4	9 - Test fails with error 9
4	4 - Test executing

REMOTE DIAGNOSTIC INTERFACE

The DS may be controlled via the Remote Diagnostics Interface (RDI) which is a hardware interface to the LEDs, board reset, and switches. The RDI echoes the information on the LEDs. It may be used to drive the board reset and also the diagnostic switches signal level “High” or “Low”. To use the RDI all diagnostic switches must be in the “OFF” state.

PC APPLICATION INTERFACE

The PCA gives the PC the capability to control the SDC master. The following operations may be carried out from the PC:

- Control of level 0 sequences
- Set up of intelligent boards interrupt level
- Retrieval of intelligent boards identity.

FUNCTIONAL DESCRIPTION

The DS consists of a number of test procedures, some available only in test mode, others performed in start-up as well as test mode.

Each of the tests is identified by a unique number.The table below is a list of the tests, describing the mode or modes in which they may be executed.

Test Sequences

Test No. (Hex)	Test Description	Start-up	Run-To-Run	Selected
01	Microcontroller Confidence and EPROM Sum Test	X	X	X
02	SRAM Data Test	X	X	X
03	SRAM Address Test	X	X	X
04	All RAM Data Test			X
05	All RAM Address Test			X
06	Serial Bus Transmit Utility			X
07	Serial Bus Receive Utility			X

Start-Up Mode

Master Node Start-Up

Start-up is selected on a master node by setting all the switches off and performing a system reset. The following sequence is then executed:

- Issue a Reset of 260 ms to the SDC Bus
- Check for PCA control request
- Check for test mode:
- Execute the following tests:
  - Test 01H Microcontroller (MCU), Confidence and EPROM Checksum Test
  - Test 02H SRAM Data Test
  - Test 03H SRAM Address Test
- Clear all SRAM to zero. (Note SRAM is not NVRAM)
- Clear all MCU RAM to zero
- Pass control to the application firmware by a “Jump” to DCX-Entry-Point procedure.

Execution time for Master Node Start-up is 16 seconds max.

Slave Node Start-Up

Start-up is selected on a slave node by setting switch SW8 off and performing a system reset. The following sequence is then executed:

- Call Initialization_Code
- Execute Test 01H
- Execute Test 02H and Test 03H
- Clear all SRAM to zero. (Note SRAM is not NVRAM)
- Pass control to the application firmware by a “Jump” to DCX-Entry-Point procedure.

Execution time for Slave Node Start-up is 15 seconds max.

Initialization_Code is called to reset all peripheral circuits on the Slave SDC node to their idle states. Initialization_Code is hardware dependent and only runs for 1 second maximum.

Both the above procedures are executed from register bank ONE.

Test Mode

This mode is selected by setting SW8 ON and performing a reset. In Test mode the settings of SW1-SW7 are also important, these switches define which test option is performed.

These options are:

- Selected Test
- Run-to-Run

Selected Test

Any test may be selected to run on its own. This is the only way in which NVRAM may be tested, or a test requiring operator intervention executed, for example, external device connection.

Run-To-Run

The purpose of Run-to-Run is to exercise as much of the Serial Bus Control electronics as possible without need of turnaround plugs or operator intervention. It will run “on” or “off” system. The sequence of tests in Run-to-Run may be run once or continuously.

Execution time for Run-to-Run is 15 seconds.

TEST DESCRIPTIONS

The following subsections define each test in turn. Each subsection also shows the switch settings which will cause the test to be executed.

TEST ROUTER

Purpose

The Test Router controls the way in which the Level 0 Diagnostics executes.

Description

- SDC Master Node
  - On power-up issue a 260 msec reset to all slave nodes on the SDC link
  - Check Register Bank 0
  - Read level 0 switches and check for PC control or execute the appropriate test or test sequence
- SDC Slave Node
  - Check Register Bank 0
  - Read level 0 switches and execute the appropriate test or test sequence.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Start-Up	X	X	X	X	X	X	X	X

Test Results

LED	**Status**
00	Start-up Passed
0D	Bad Switch Setting
0E	CPU Quick Check Failed

NOTE: If the LEDs indicate 0FH then the MCU is probably held in “Reset” type state.

TEST 01H - MICRO-CONTROLLER CONFIDENCE AND EPROM SUMCHECK

Purpose

To test the Micro-Controller, MCU and check that the contents of the EPROM is valid.

Description

The following functions are performed:

- Check the required MCUcommands, flags and registers needed to perform a sumcheck on the EPROM
- Perform EPROM sumcheck
- Perform Internal RAM checking - using rolling ones technique
- Check remaining MCU commands, flags and registers
- Test micro-controller internal functions
  - Timers
  - Interrupt Control Registers
  - Serial Channel.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Start-up:								
Master Node	0	0	0	0	0	0	0	0
Slave Node	X	X	X	X	X	X	X	0
Run-To-Run	0	0	0	0	0	SW6	SW7	1
Selected	0	0	0	0	0	SW6	SW7	1

Test Results

LED	**Status**
00H	Pass
08H	MCU ALU fault
09H	MCU RAM fault
0AH	MCU timer fault
0BH	MCU interrupt control register fault
0CH	MCU serial control register fault
0DH	EPROM sumcheck fail

Notes

The following bytes in EPROM are reserved for L0 diagnostics.

PROM Type	**16K x 8 (27128)**	**32K x 8 (27256)**	**64K x 8 (27512)**
Reserved	03FFBH	07FFBH	0FFFBH
(to be set to zero)	03FFCH	07FFCH	0FFFCH
	03FFDH	07FFDH	0FFFDH
EPROM Sumcheck	03FFEH	07FFEH	0FFFEH
	03FFFH	07FFFH	0FFFFH

TEST 02H - SRAM DATA

Purpose
To test all SRAM not allocated as non volatile RAM, NVRAM.

Description
The following sequence is executed:

1. SRAM data area boundaries are calculated as follows:
   Check for NVRAM area check bytes -

Location	Byte
0FFFFH	0AAH
0FFFEH	055H
0FFFDH	000H
0FFFCH	0FFH
0FFFBH	High byte of NVRAM base
0FFFAH	Low byte of NVRAM base

   Check locations 08000H and 08001H for presence of 2nd SRAM device.
2. First two bytes of SRAM under test checked for any faults external to SRAM
3. A 1 is rotated through each byte in SRAM under test to check for internal SRAM faults.

Test Selection

Test Mode	<---------- Switch Setting ---------->							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Start-up:								
Master Node	0	0	0	0	0	0	0	0
Slave Node	X	X	X	X	X	X	X	0
Run-To-Run	0	0	0	0	0	SW6	SW7	1
Selected	0	1	0	0	0	SW6	SW7	1

Test Results

LED	Status
00H	Pass
08H	Internal SRAM data error in lower SRAM
09H	Internal SRAM data error in upper SRAM
0AH	External data fault on lower SRAM
0BH	External data fault on upper SRAM

Notes
If board is populated with only one SRAM then error codes refer to upper or lower half of tested memory.

TEST 03H - SRAM ADDRESS

Purpose

To check that there are no hard faults on memory not allocated as NVRAM.

Description

The following sequence is executed:

1. Calculate SRAM boundaries as per Test 02H
2. Write 00H to all SRAM under test and verify
3. Write 0FFH to Byte 0 of SRAM under test and verify
4. Read back from locations given by enabling one and only one address line. These are the diagonal addresses (1,2,4,8...). If an address line fails to all of SRAM under test, then data read back is 0FFH. If an address fails internally to one bit of SRAM, then data read back is neither 00H or 0FFH.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Start-up:								
Master Node	0	0	0	0	0	0	0	0
Slave Node	X	X	X	X	X	X	X	0
Run-To-Run	0	0	0	0	0	SW6	SW7	1
Selected	1	1	0	0	0	SW6	SW7	1

Test Results

LED	**Status**
00H	Pass
08H	Data error while verifying 00H write
09H	Data error while verifying 0FFH write
0AH	Lower SRAM address bus error in lower 8 lines BA0-7
0BH	Lower SRAM address bus error in upper 8 lines BA8-15
0CH	Upper SRAM address bus error in lower 8 lines BA0-7
0DH	Upper SRAM address bus error in upper 8 lines BA8-15

Notes

If board is populated with only one SRAM then error codes refer to upper or lower half of memory.

TEST 04H - ALL RAM DATA

Purpose

This test has the same purpose as Test 02H except that all populated RAM is tested.

CAUTION

This test will destroy any data stored within RAM area located as NVRAM.

Description

As per Test 02H except that Step 1 is missed and all populated RAM is tested.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Selected	0	0	1	0	0	SW6	SW7	1

Test Results

LED	**Status**
00H	Pass
08H	Internal data fault in lower SRAM
09H	Internal data fault in upper SRAM
0AH	External data fault on lower SRAM
0BH	External data fault on upper SRAM

Notes

If board is only populated with one SRAM then error codes refer to upper or lower half of memory.

TEST 05H - ALL RAM ADDRESS

Purpose

As in Test 03H except that all populated RAM is tested.

CAUTION

Any data held in NVRAM allocated area will be destroyed.

Description

As in Test 03H except that Step 1 is missed and all populated RAM is tested.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Selected	1	0	1	0	0	SW6	SW7	1

Test Results

LED	**Status**
00H	Pass
08H	Data error while verifying 000H write
09H	Data error while verifying 0FFH write
0AH	Lower SRAM address bus error in lower eight lines BA0-7
0BH	Lower SRAM address bus error in upper eight lines BA8-15
0CH	Upper SRAM address bus error in lower eight lines BA0-7
0DH	Upper SRAM address bus error in upper eight lines BA8-15
0EH	Chip select fault

Notes

If board is only populated with one SRAM then error codes refer to upper or lower half of memory.

TEST 06H - SERIAL BUS TRANSMIT UTILITY AND INTERNAL LOOP TEST

Purpose

To allow any SDC node to become a transmitting master and transmit a 21 byte test pattern.

Description

The SDC node selected as the transmitting master executes the following sequence:

1. Delay for 130 milliseconds
2. Transmit the following test pattern:
   One wake up byte, 077H with 9th bit set, followed by a 20 byte data train:

   E7,7E,3E,81,AA,00,55,51,FF,BC,CD,18,46,99,22,F7,10,6C,CF,20H

3. Check transmission time. The link is set up to run at 375 kbps in polled mode.

Test Selection

Test Mode	**<---------- Switch Setting ----------->**							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Selected	0	1	1	0	0	SW6	SW7	1

Test Results

LED	**Status**
06H	Test running (This test does not return a status unless it fails).
0AH	Timing problem during transmission or data unable to be transmitted.
0BH	Incorrect byte received from turnaround.

Notes

Only one SDC node can be the transmitting master at any one time.

TEST 07H - SERIAL BUS RECEIVE UTILITY

Purpose

To allow any SDC node to become a slave receiver and receive a 21 byte test pattern.

Description

The following sequence is executed:

1. Wait one second for start of test pattern.
2. Receive the test pattern as detailed in Test 06H.
3. Check reception time.

Test Selection

Test Mode	<---------- Switch Setting ---------->							
Slave Node	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8
Master Node	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16
Selected	1	1	1	0	0	SW6	SW7	1

Test Results

LED	Status
07H	Test running (This test does not return a status unless it fails)
09H	Serial control register or power control register not verifying.
0AH	Data byte not received or power control register fault.
0BH	Incorrect data byte received.

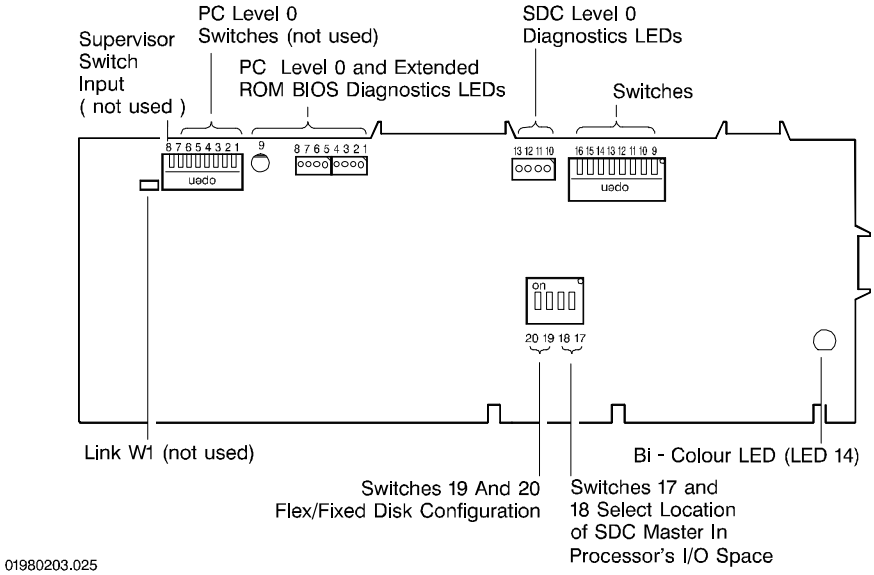
Notes

Test 06H must be running on another node on the link before this test is started.

Any number of slave devices can run this test at one time.

STRAPPING

The following illustration shows the position of the strapping on the SSPM and the table shows the default position of the straps and switches on the SSPM board:



NOTE: Bicolour LED 14 is numbered LED 5 on the PCB screen printing.

Strap	Purpose	Normal Position
W1	Supervisor switch input	Not used
SW1	Clears system NVRAM on reset or power up (SEE CAUTION)	Open
SW2	Reserved for PC level 0 diagnostic test selection	Not used
to		Set to Open
SW7		
SW8	Supervisor switch input	Not used - set to Open
SW9	SDC level 0 diagnostic test selection	Set to Open
to		
SW16		
SW17)	Selects position of SDC Master in processor's I/O space at	On
SW18)	port 0200H - 020FH	On
SW19)	Selects flex controller at primary address and configures fixed	Off
SW20)	disk	Off

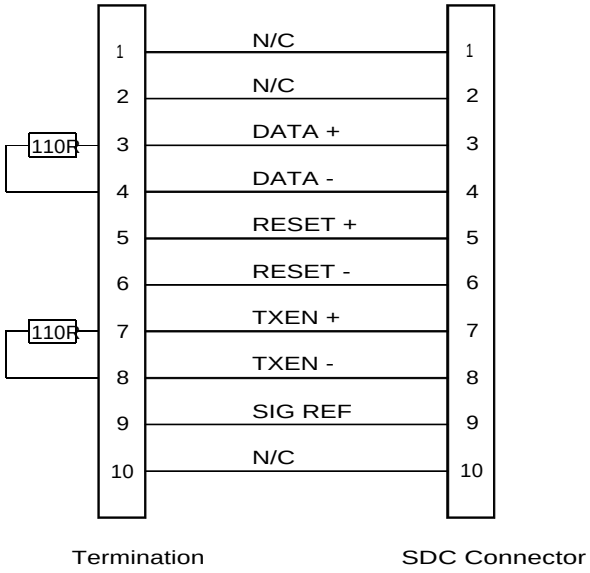
NOTE: The positions "Open" and "On" are marked on the switch packs on the board. Open = Off = logic 0, Closed = On = logic 1.

CAUTION

Set switch 1 only as a last resort! All system NVRAM (logs, tallies, application counters) will be cleared.

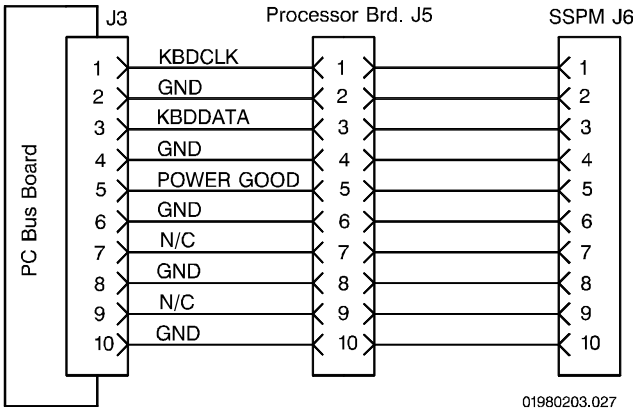
CABLE INFORMATION

SDC BUS HARNESS

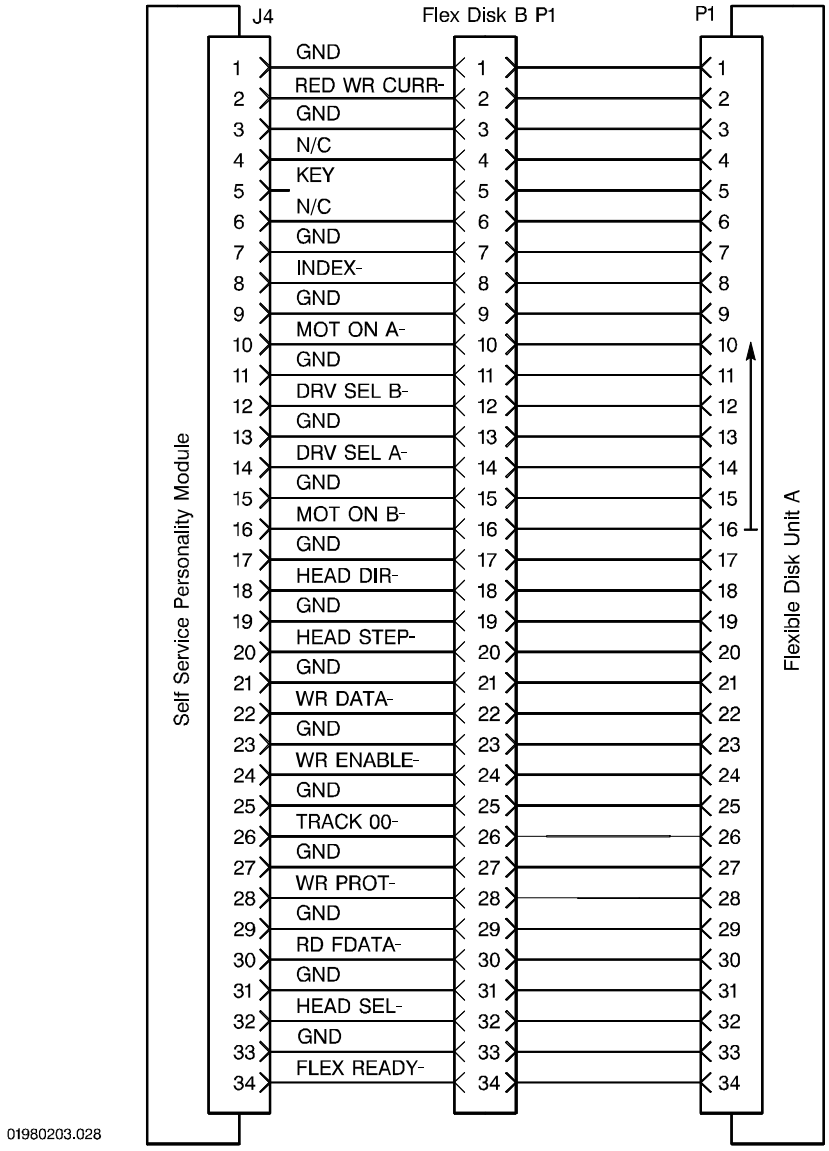


POWER GOOD HARNESS

The following figure shows the path of the power good signal via the PC busboard harness to connector J6 on the SSPM;



FLEXIBLE DISK UNITS HARNESS



CONNECTOR ASSIGNMENT

GRAPHICS INTERFACE CONNECTOR (J1)

This is a 62-way (2 x 31) connector. The signals on this connector are taken directly from the PC bus connection a and b.

Pin	*a*	*b*
1	IOCHK/	GND
2	SD7	RESETDRV
3	SD6	+5 VOLTS
4	SD5	IRQ2/9
5	SD4	-5 VOLTS
6	SD3	DRQ2
7	SD2	-12 VOLTS
8	SD1	OWS
9	SD0	+12 VOLTS
10	IOCHRDY	GND
11	AEN	SMEMW/
12	SA19	SMERW/
13	SA18	IOW/
14	SA17	IOR/
15	SA16	DACK3/
16	SA15	DRQ3/
17	SA14	DACK1/
18	SA13	DRQ1
19	SA12	REFRESH/
20	SA11	CLK
21	S10	IRQ7
22	SA9	IRQ6
23	SA8	IRQ5
24	SA7	IRQ4
25	SA6	IRQ3
26	SA5	DACK2/
27	SA4	T/C
28	SA3	BALE
29	SA2	+5 VOLTS
30	SA1	OSC
31	SA0	GND

CONNECTOR (J2)

This connector is not populated on the board. It repeats the signals on the 16-bit bus extension connector.

MEMORY EXPANSION INTERFACE CONNECTOR (J3)

This is 62-way (2 x 31) connector. The signals on this connector are taken directly from the PC bus edge connectors.

Pin	*e*	*f*
1	IOCHK/	GND
2	SD7	RESETDRV
3	SD6	+5 VOLTS
4	SD5	SBEH/
5	SD4	LA23
6	SD3	LA22
7	SD2	LA21
8	SD1	LA20
9	SD0	LA19
10	N/C	GND
11	N/C	SD8
12	N/C	SD9
13	SA18	SD10
14	SA17	SD11
15	SA16	SD12
16	SA15	SD13
17	SA14	SD14
18	SA13	SD15
19	SA12	REFRESH/
20	SA11	MEMR/
21	S10	MEMW/
22	SA9	MEMCS16/
23	SA8	N/C
24	SA7	N/C
25	SA6	N/C
26	SA5	N/C
27	SA4	N/C
28	SA3	BALE
29	SA2	+5 VOLTS
30	SA1	N/C
31	SA0	GND

FLEX DISK INTERFACE CONNECTOR (J4)

This is a 34-way (2 x 17) connector. All odd numbered pins are grounded.

GND	1	2	Write Current Control
GND	3	4	N/C
GND	5	6	N/C
GND	7	8	Index
GND	9	10	Motor A Enable
GND	11	12	Drive B Select
GND	13	14	Drive A Select
GND	15	16	Motor B enable
GND	17	18	Direction
GND	19	20	Step
GND	21	22	Write Data
GND	23	24	Write Gate
GND	25	26	Track 00
GND	27	28	Write Protect
GND	29	30	Read Data
GND	31	32	Side 1 Select
GND	33	34	Ready/Media Change

SDC MASTER REMOTE LEVEL 0 INTERFACE CONNECTOR (J5)

This is a 20-way (2 x 10) connector of stake pins. Pin 1 is the top left hand corner of the array.

+5 VOLTS	1	2	RESET/
SWITCH 9	3	4	N/C
SWITCH 10	5	6	LED10
SWITCH 11	7	8	LED11
SWITCH 12	9	10	KEY
SWITCH 13	11	12	LED12
SWITCH 14	13	14	LED13
SWITCH 15	15	16	N/C
SWITCH 16	17	18	N/C
GND	19	20	GND

POWER GOOD CONNECTOR (J6)

This is a 10-way connector daisy-chained from the 80286 (Marie Curie) Processor Board. On the SSPM only the power-good signal is picked up.

N/C	1	2	N/C
N/C	3	4	N/C
POWER - GOOD	5	6	N/C
N/C	7	8	N/C
N/C	9	10	N/C

SDC LINK CONNECTORS

Local Link Connector (J7)

J7 is a 10-way (2 x 5) connector mounted on the SSPM board. It is intended for connection to SDC secondary devices which are plugged into the Bus Board.

N/C	1	2	N/C
DATA+	3	4	DATA-
RESET+	5	6	RESET-
KEY	7	8	N/C
SIGREF	9	10	+5V

Remote Link Connector (J8)

J8 is a 10-way (2 x 5) connector mounted on the SSPM board. It is intended for connection to SDC secondary devices which are located outside the card cage.

N/C	1	2	N/C
DATA+	3	4	DATA-
RESET+	5	6	RESET-
TX EN+	7	8	TX EN-
SIGREF	9	10	N/C

SUPERVISOR SWITCH CONNECTOR (J10)

This is a 3-way right angled header connector with the following pinout:

SWITCH 8	1
N/C	2
GND	3

SCHEMATIC DIAGRAMS

The following fold out pages contain the schematic diagrams for the Self Service Personality Module and for a Secondary Node.

- Schematic 445-0589572 on pages FO-1 to FO-8 applies to SSPM assemblies:
  - 445-0589570 - Secure SSPM
  - 445-0589550 - Standard Secure SSPM
  - 445-0593250 - Secure SSPM
  - 445-0593240 - Standard Secure SSPM
- Schematic 445-0598822 on pages FO-9 to FO-16 applies to SSPM assemblies:
  - 445-0598820 - Secure SSPM
  - 445-0598830 - Standard Secure SSPM
- Schematic 445-0582599 on pages FO-17 to FO-19 applies to SDC secondary nodes.