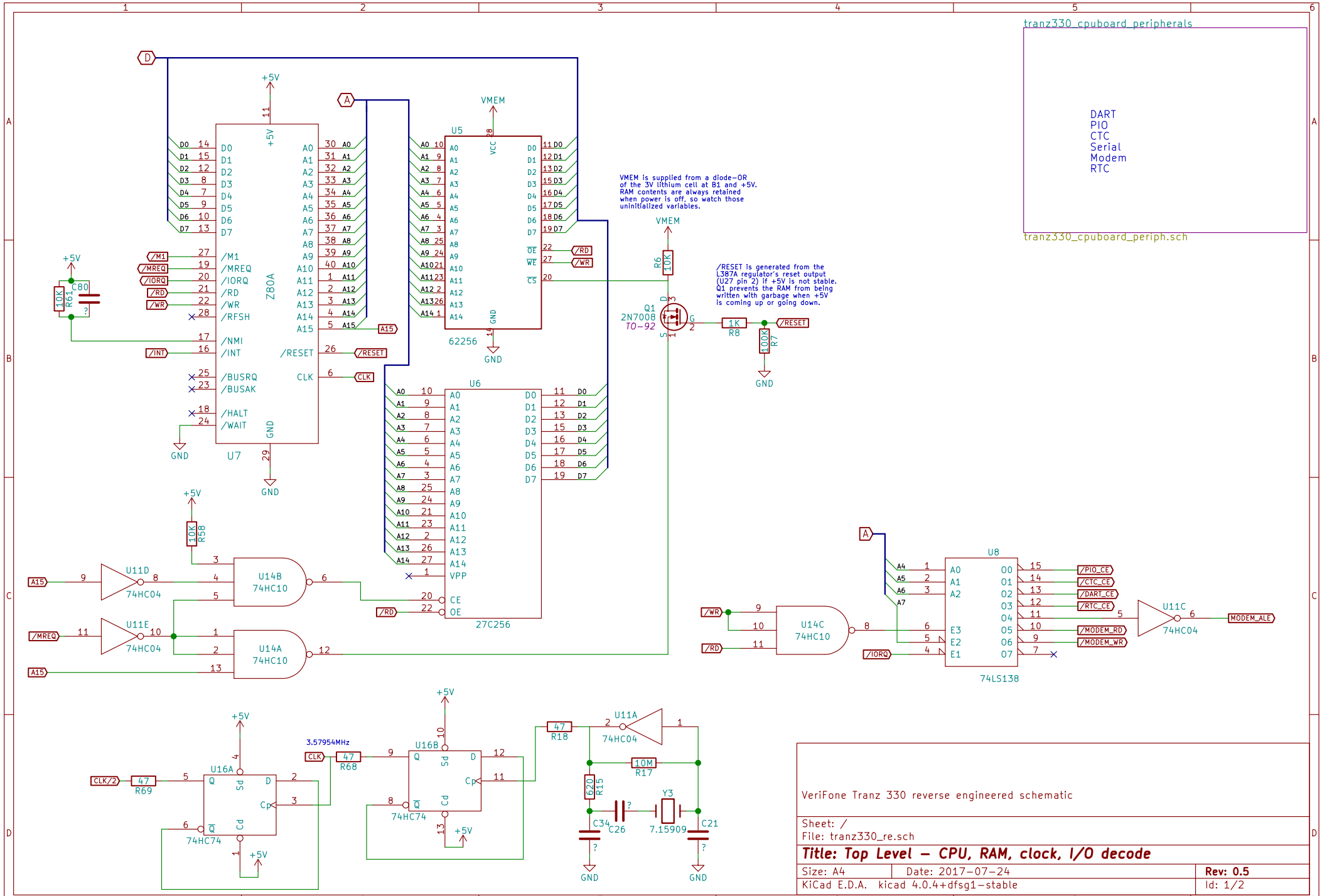
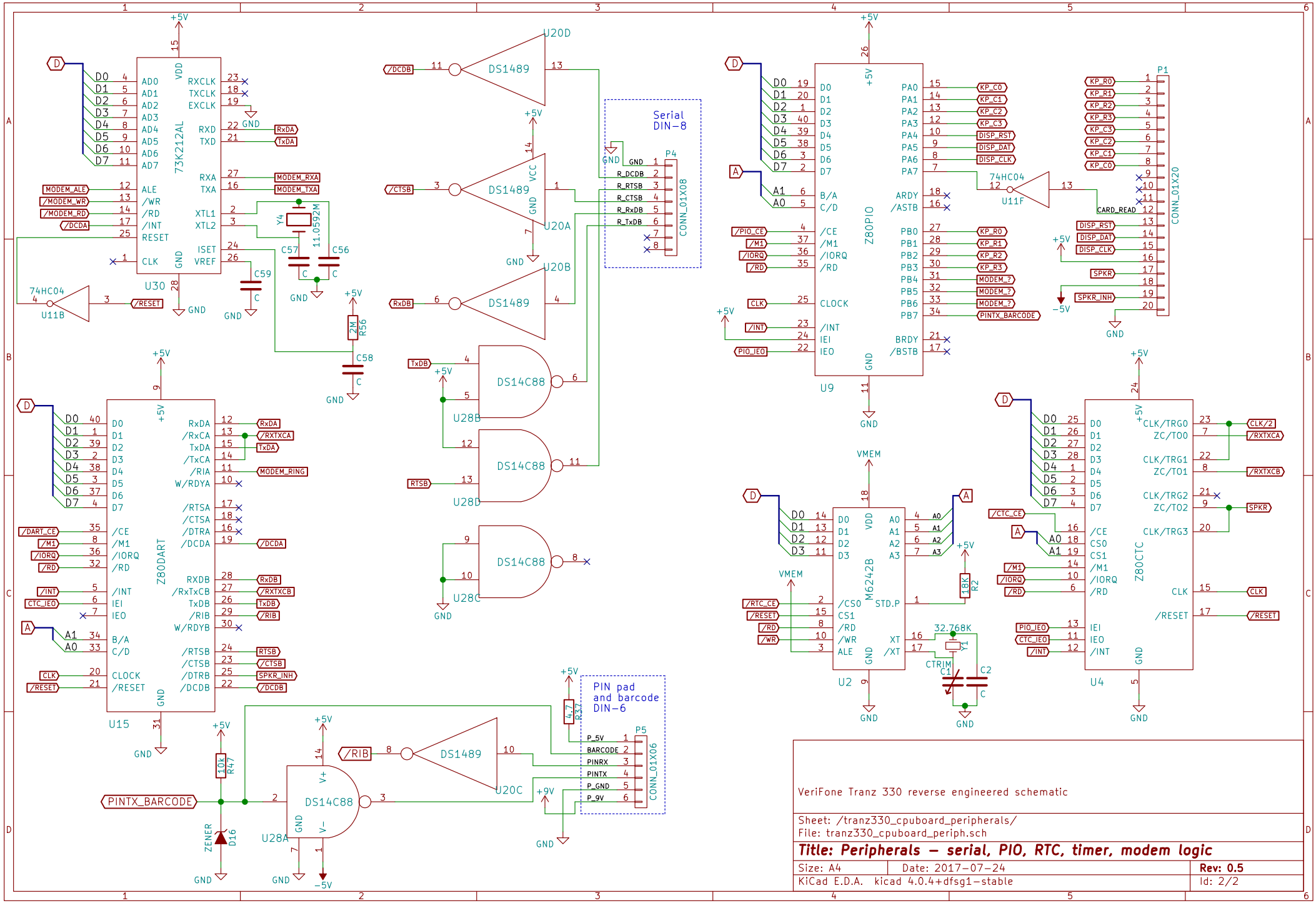

tranz330_cpuboard_peripherals
DART
PIO
CTC
Serial
Modem
RTC
tranz330_cpuboard_periph.sch
U7
Z80A
U5
62256
U6
27C256
VMEM is supplied from a diode-OR of the 3V lithium cell at B1 and +5V. RAM contents are always retained when power is off, so watch those uninitialized variables.
/RESET is generated from the L387A regulator's reset output (U27 pin 2) if +5V is not stable. Q1 prevents the RAM from being written with garbage when +5V is coming up or going down.
Q1
2N7008
TO-92
R6 10K
R8 1K
R7 100K
R61 10K
C80
R58 10K
U14B 74HC10
U14A 74HC10
U14C 74HC10
U11D 74HC04
U11E 74HC04
U11C 74HC04
U11A 74HC04
U8
74LS138
/PIO_CE
/CTC_CE
/DART_CE
/RTC_CE
/MODEM_RD
/MODEM_WR
MODEM_ALE
U16A
U16B
74HC74
3.57954MHz
R69 47
R68 47
R18 47
R17 10M
R15 620
C34
C26
Y3
7.15909
C21
VeriFone Tranz 330 reverse engineered schematic
Sheet: /
File: tranz330_re.sch
Title: Top Level – CPU, RAM, clock, I/O decode
Size: A4
Date: 2017-07-24
Rev: 0.5
KiCad E.D.A. kicad 4.0.4+dfsg1-stable
Id: 1/2


U30
73K212AL
U11B
74HC04
Y4
11.0592M
C57
C56
C59
C58
R56
2M
U20D
U20A
U20B
DS1489
Serial
DIN-8
P4
CONN_01X08
U28B
U28D
U28C
DS14C88
U9
Z80PIO
U11F
P1
CONN_01X20
U15
Z80DART
U2
M6242B
Y1
32.768K
R2
18K
U4
Z80CTC
U28A
U20C
R47
10K
D16
ZENER
R37
4.7
PIN pad
and barcode
DIN-6
P5
CONN_01X06
PINTX_BARCODE
VeriFone Tranz 330 reverse engineered schematic
Sheet: /tranz330_cpuboard_peripherals/
File: tranz330_cpuboard_periph.sch
Title: Peripherals – serial, PIO, RTC, timer, modem logic
Size: A4
Date: 2017-07-24
Rev: 0.5
KiCad E.D.A. kicad 4.0.4+dfsg1-stable
Id: 2/2