Depletion/Enhancement CMOS For a Low Power Family of Three-Valued Logic Circuits

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Abstract—A new family of ternary logic circuits that uses both depletion and enhancement types of complementary metal-oxide semiconductor (CMOS) transistors is presented. These circuits use two power supplies each below the transistor's threshold voltages and do not include resistors. Circuit designs of basic ternary operators (inverters, NAND, NOR) are described. These basic ternary operators can be used as building blocks in the VLSI implementation of three-valued digital systems. An example of the design of a ternary full adder using this family of logic circuits is also presented.

I. Introduction

THE complementary metal-oxide semiconductor (CMOS) family of integrated circuits has been used by several authors in the realization of three-valued logic circuits [1]–[8]. In all previous designs, these authors have used voltage power supplies higher than the threshold voltage of the p- and n-channel MOS transistors. In most cases, this has resulted in high power consumption in the circuits. Recently, a new family of three-valued CMOS circuits that is not restricted to the use of power supplies at the above threshold voltages has been reported [9] and applied to the design of an all-CMOS ternary computer [10]. The new design [9], [10] reduces power consumption in the circuits. In order to further reduce the power consumption as well as increase the speed of these circuits, a new design that does not use resistors at all is needed. Such a design would be extremely useful in the VLSI implementation of three-valued digital systems. This paper is an attempt to respond to this need, consolidating ideas initially presented at ISMVL-84 [11].

In this paper, the design of a new family of ternary logic circuits based on the use of depletion enhancement complementary metal-oxide-semiconductor (DECMOS) integrated circuits is presented. The circuits use two power supplies each below the transistors' threshold voltage and do not require resistors. The circuit design of basic ternary operators (inverters, NAND, NOR) is described. An example of the use of these basic ternary operators as building blocks in the design of a ternary full adder is also presented.

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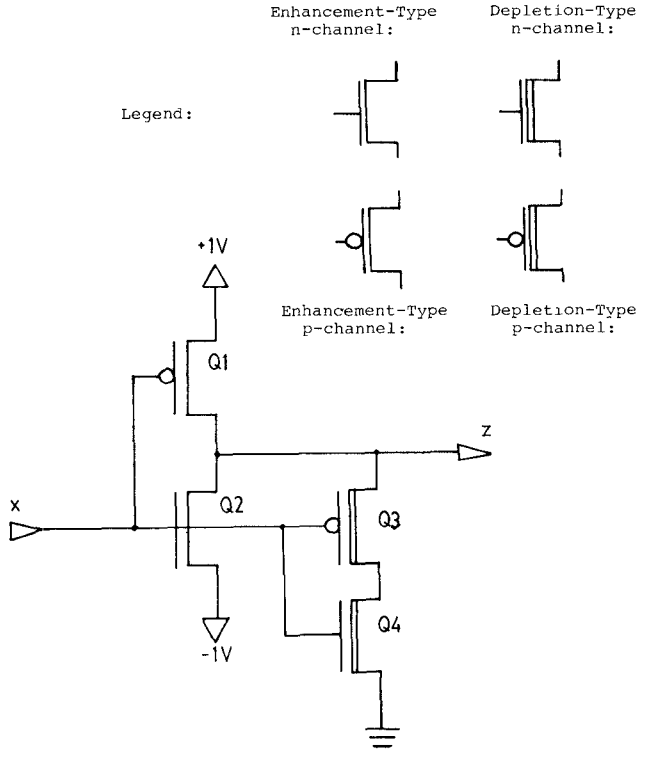

Fig. 1. Simple Ternary Inverter.

II. Design Description

The Simple Ternary Inverter (STI), the Positive Ternary Inverter (PTI), and the Negative Ternary Inverter (NTI) are the three unary operators considered in this system [2]. The STI is composed of one of each of a p-channel and n-channel enhancement-type and a p-channel and n-channel depletion-type MOS transistors connected as shown in Fig. 1. The source of the p-channel enhancement-type transistor (Q_1) is connected to a +1-V power supply and the source of the n-channel enhancement-type transistor (Q_2) is connected to −1 V. The drains of the two channels are connected to each other and constitute the output that is also connected to the drain of a p-channel depletion-type transistor (Q_3). The source of transistor Q_3 is connected to the drain of an n-channel depletion-type transistor (Q_4) whose source is connected to the ground. The gates of the four transistors are connected together to the input x.

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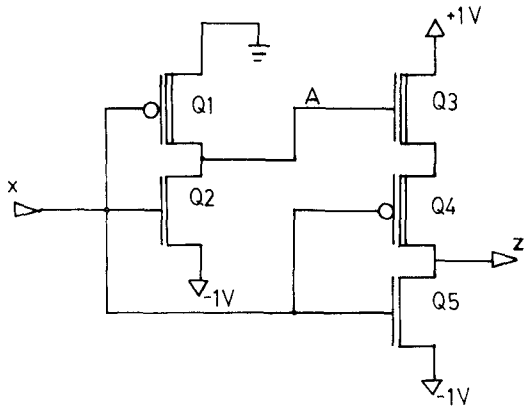

Fig 2. Positive Ternary Inverter.

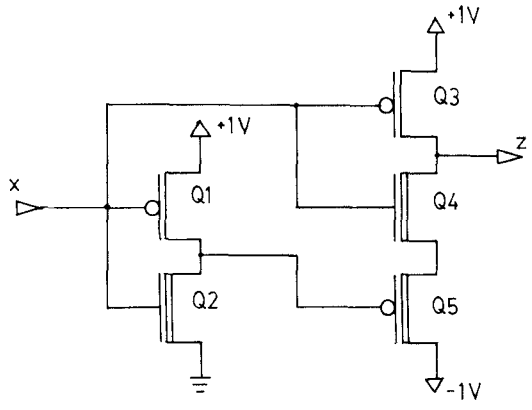

Fig. 3. Negative Ternary Inverter.

TABLE I
DECMOS POWER CONSUMPTION, RISE AND FALL TIME

Gate	Power consumption	rise time			fall time		
		-1 → 0	0 → 1	-1 → 1	1 → 0	0 → -1	1 → -1
STI	9.02 pW	10ns	10ns	18ns	5ns	10ns	13ns
PTI	15.00 pW	--	--	70ns	--	--	13ns
NTI	15.00 pW	--	--	15ns	--	--	70ns
TNAND	11.00 pW	15ns	25ns	25ns	25ns	20ns	25ns
TNOR	18.00 pW	15ns	40ns	55ns	25ns	15ns	15ns

TABLE II
DECMOS NOISE MARGIN CHARACTERISTICS

Gate	Noise Margin					
	1 → 0	0 → 1	0 → -1	-1 → 0	1 → -1	-1 → 1
STI	0.4V	0.4V	0.4V	0.45V	--	--
PTI	--	--	--	--	0.1V	0.45V
NTI	--	--	--	--	0.45V	0.1V
TNAND	0.4V	0.3V	0.4V	0.4V	--	--
TNOR	0.3V	0.4V	0.35V	0.35V	--	--

Following one of many possible conventions, we shall label the lower, middle, and upper levels logic -1, 0, and 1, respectively. Thus the STI is defined by [1], [2]

$$\overline{x^0} = -x \tag{1}$$

where the minus sign represents arithmetic negation.

If the input x is at the high level (logic 1), transistor Q_1 will be off while transistor Q_2 will be on. At the same time, Q_3 will be off even though Q_4 will be on which will keep the output on the low level (logic -1). The output will be at logic 1 if the input x is at logic -1 because in this case Q_1 and Q_3 are on but Q_2 and Q_4 are off. However, if the input x is at the intermediate level (logic 0), both enhancement-type transistors Q_1 and Q_2 will be off but depletion-type transistors Q_3 and Q_4 will be on which will force the output to be at the ground voltage level (logic 0).

Note that, for proper operation of the above STI circuit the following relationship must be satisfied:

$$V < V_T < 2\text{ V} \tag{2}$$

$$0 < V_P < V \tag{3}$$

where $\pm V$ is the value of the power supply and V_T is the threshold voltage of the p-channel and/or n-channel enhancement MOS transistors, while V_P is the pinchoff voltage of the p-channel and/or n-channel depletion devices.

The Positive Ternary Inverter uses five transistors connected as shown in Fig. 2. The source of a p-channel depletion-type transistor (Q_1) is connected to the ground and the source of an n-channel enhancement-type transistor (Q_2) is connected to a -1-V power supply. The drains of the two channels are connected to each other and the gate of a third transistor (Q_3) of the n-channel depletion-type. The source of Q_3 is connected to $+1$ V while its drain is connected to the source of a fourth transistor (Q_4)

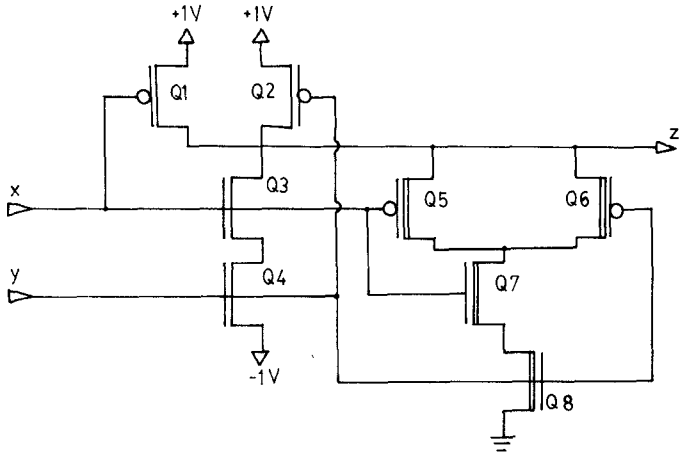

Fig. 4 Ternary NAND gate.

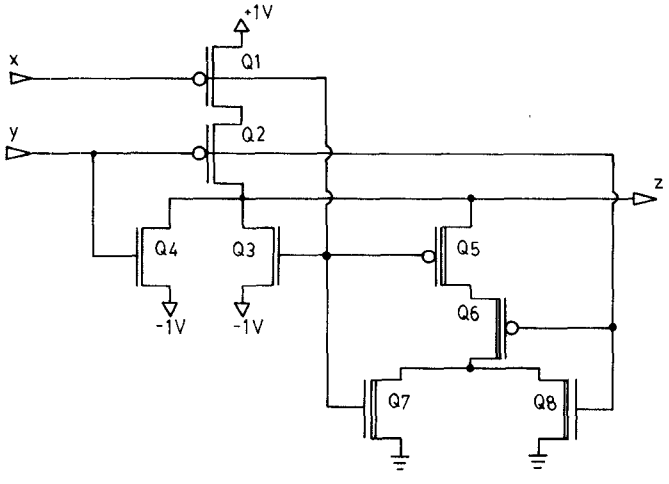

Fig. 5. Ternary NOR gate.

of the p-channel depletion-type. The drain of Q_4 is connected to the drain of an n-channel enhancement-type transistor (Q_5) and constitutes the output of this PTI circuit. The source of Q_5 is connected to -1 V and its gate as well as the gates of transistors Q_1, Q_2, and Q_4 are connected to the input x.

If the input x is at logic 1, transistor Q_1 will be off while transistor Q_2 will be on, making point A -1 V which will force transistor Q_3 to be off. At the same time transistor Q_4 will be off while transistor Q_5 will be on. Thus the output will be at logic -1. However, if the input is at logic -1 transistors Q_1, Q_3, and Q_4 will be on while transistors Q_2 and Q_5 will be off forcing the output to be at logic 1. The output will also be at logic 1 if the input x is at logic 0 because the depletion-type transistors Q_1, Q_3, and Q_4 will be on while the enhancement-type transistors Q_2 and Q_5 will be off.

Similarly, the NTI circuit is designed with five transistors as shown in Fig. 3. Two enhancement-type p-channel transistors Q_1 and Q_3, two depletion-type n-channel transistors Q_2 and Q_4, and one depletion-type p-channel transistor Q_5 are connected in a dual form of the PTI circuit described above. In this case, when the input x is at logic 1 or logic 0 transistors Q_1 and Q_3 are off while transistors Q_2, Q_4, and Q_5 are on forcing the output to be at logic -1. However, the output will be at logic 1 if the input is at logic -1 because transistors Q_1 and Q_3 are on while transistors Q_2, Q_4, and Q_5 are all off.

The function of the PTI and NTI can be defined by

$$\overline{x^i} = \begin{cases} i, & \text{if } x = 0 \\ -x, & \text{if } x \neq 0 \end{cases} \tag{4}$$

where i takes the value of 1 for the PTI and -1 for the NTI operator.

The ternary NAND and ternary NOR are two multiple entry operators used in this system [2]. The functions of the two-entry ternary NAND and ternary NOR are defined by the following two equations, respectively,

$$\overline{X \wedge Y^0} = \overline{\min(X, Y)^0} \tag{5}$$

$$\overline{X \vee Y^0} = \overline{\max(X, Y)^0}. \tag{6}$$

The circuits for the 2-input ternary NAND and ternary NOR are shown in Figs. 4 and 5, respectively. They are essentially the same as their binary counterpart except for the different power supplies and the additional depletion mode devices connected to their inputs and centering the output. In these two circuits, transistors Q_1–Q_4 are of the enhancement type and transistors Q_5–Q_8, which have the same configuration as Q_1–Q_4 circuit, are of the depletion type. The gates of transistors Q_1 and Q_3 (enhancement) and transistors Q_5 and Q_7 (depletion) are connected as are the gates of transistors Q_2 and Q_4 (enhancement) and transistors Q_6 and Q_8 (depletion). In these two circuits the function of the depletion-type transistors is to pull the output to the intermediate logic level (0 V) when necessary. The reader can apply the argument used in the STI case to see that these circuits actually perform the desired logic functions. For example, if inputs X and Y are logic 0 and 1 then the outputs of the ternary NAND and ternary NOR will be logic 0 and -1, respectively, because in both cases transistors Q_1, Q_2, Q_3, and Q_6 are off while transistors Q_4, Q_5, Q_7, and Q_8 are on.

It has to be noted here that (2) and (3) hold as a condition for proper operation also in the case of PTI, NTI, ternary NAND, and ternary NOR circuits.

III. Performance

The performance of all the above circuits has been studied using the SPICE 2G Simulation package. All transistor sizes are 5 μm$\times$5 μm. The threshold voltages of the p-channel and n-channel enhancement-type transistors are -1 and $+1$ V, respectively, while for the depletion-type transistors they are $+1$ and -1 V, respectively. The voltage power supplies are as shown on all figures $+1$, 0, and -1 V. The dc power consumption, rise time, and fall time for all of the above circuits are summarized in Table I. It has been noted that notations $-1 \rightarrow 1$ and $1 \rightarrow -1$, on Table I, are the 10–90-percent and the 90–10-percent

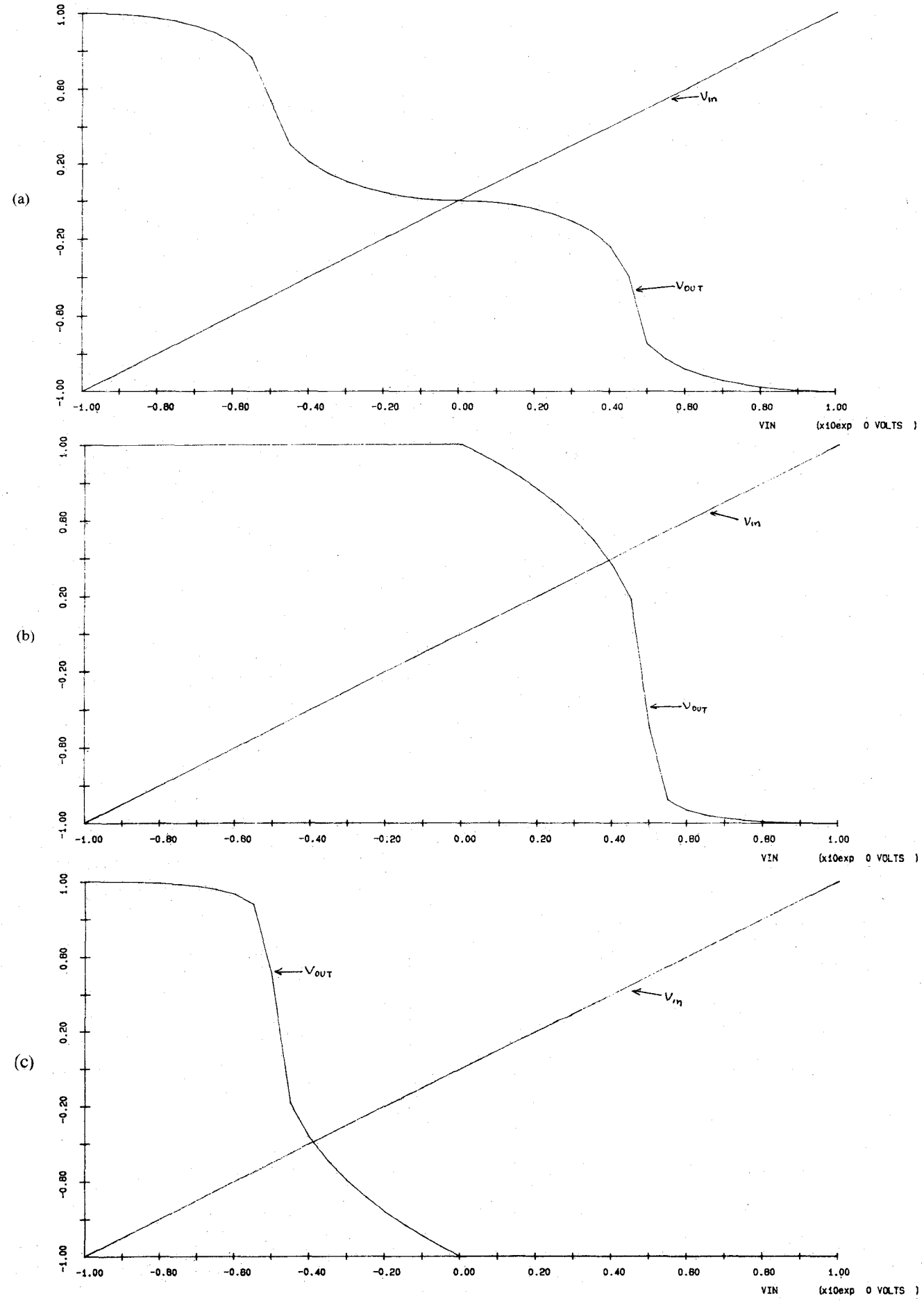

Fig. 6. Static characteristics. (a) STI. (b) PTI. (c) NTI.

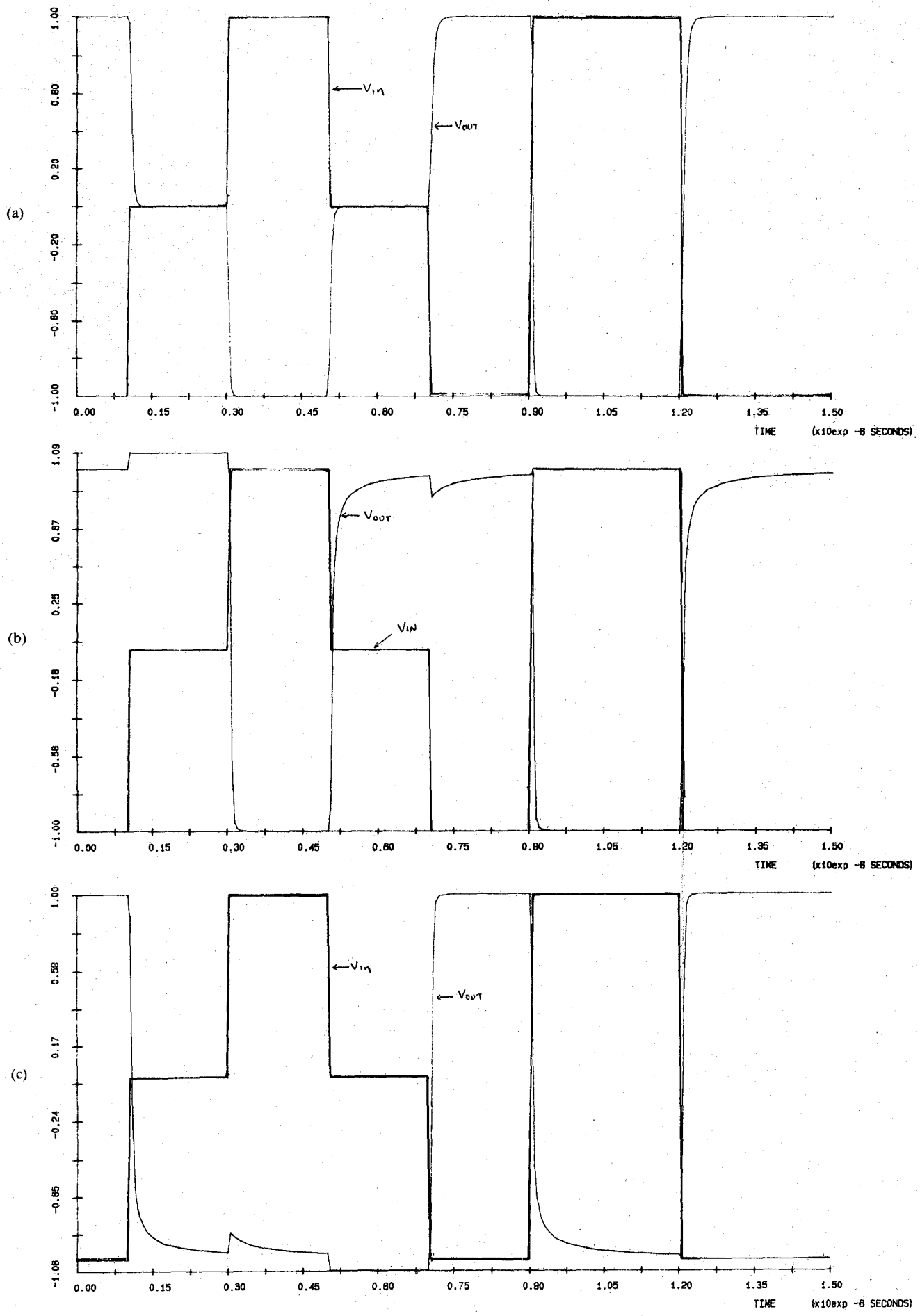

Fig. 7. Dynamic characteristics. (a) STI. (b) PTI. (c) NTI.

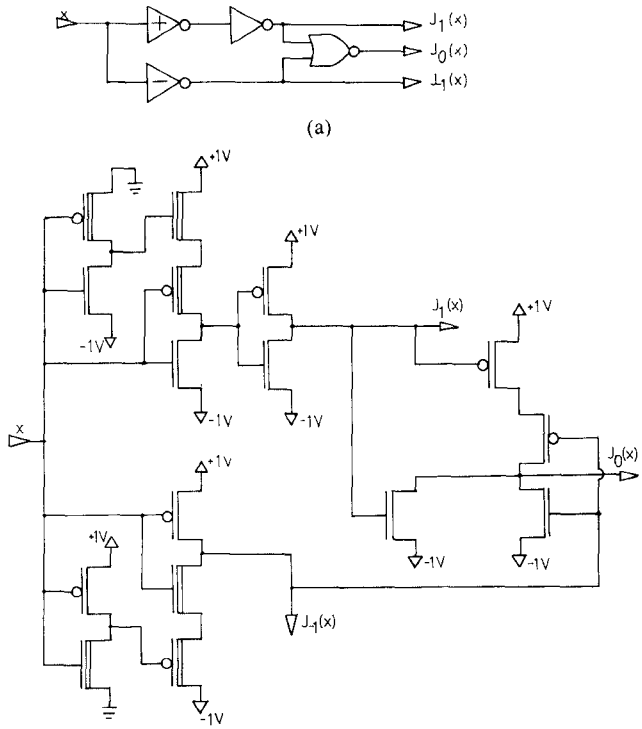

Fig. 8. J_K Arithmetic circuit. (a) Block diagram. (b) Schematic.

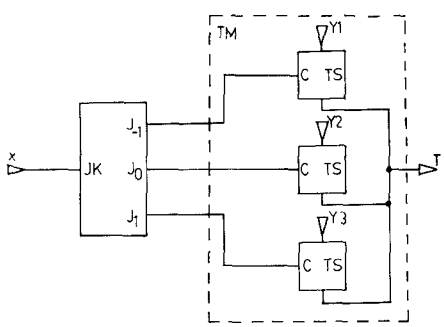

Fig. 9. Ternary T-gate.

times for a 2-V swing while notations $0 \rightarrow 1$, $1 \rightarrow 0$, $0 \rightarrow -1$, and $-1 \rightarrow 0$ are that of 1-V swing. The static and dynamic characteristics of the ternary inverter circuits are given in Figs. 6 (a)–(c) and 7 (a)–(c), respectively. As can be seen from the static characteristic curves, the circuits have very good noise margin of about 40 percent of the power supplies in most cases (Table II). It has to be noted that the rise and fall time of these circuits can be improved by reducing the length to width (L/W) ratio of the transistors used, at the expense of increased power consumption.

IV. Application: The Ternary Full Adder

Based on the DECMOS ternary operator circuitry described above, it is possible to design any arbitrary ternary digital system [2]. For illustration the design of a ternary full adder is given below. In preparation, the design of the J_K arithmetic circuit and the three-valued T-gate are first presented as they are used to construct the full adder. The

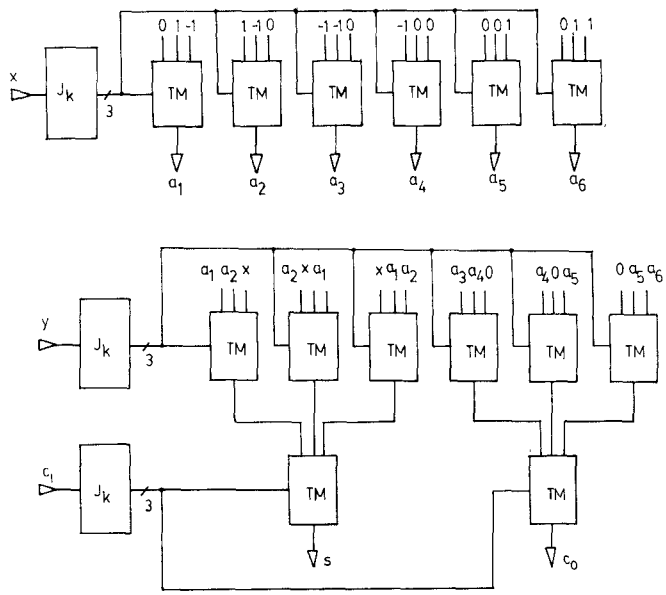

Fig. 10. Ternary full adder.

$J_K(x)$ function [12] is defined by

$$J_K(x) = \begin{cases} 1, & \text{if } x = k \\ -1, & \text{if } x \neq k \end{cases} \tag{7}$$

where k can take the values of -1, 0, or 1.

The J_K arithmetic circuit is composed of an NTI, a PTI, an STI, and a ternary NOR gate connected, as shown in Fig. 8(a) in block diagram form and in Fig. 8(b) in schematic diagram form. In Fig. 8, it can be noticed that the depletion mode circuitry of the STI and the ternary NOR has been omitted since their inputs and consequently their output are never at logic 0. This further reduces the complexity of the system.

The design of the T-gate circuit is based on the J_K arithmetic circuit described above. The function of the T-gate [13] is described by

$$T(y_1, y_2, y_3; x) = y_i \tag{8}$$

where i will equal 1 if x takes the value of -1, 2 if x is 0, and 3 if x is 1.

The block diagram of the T-gate is shown in Fig. 9. It is composed of a J_K arithmetic circuit and three ternary switches (TS). Each TS consists of one p-channel and one n-channel enhancement-type transistor. The source of the p-channel is connected to the drain of the n-channel and vice versa. A control signal C is required for proper switch operation. This signal controls the n-channel directly and the p-channel is controlled by $\overline{C^0}$. Both channels are biased on or off simultaneously by the control signal C. When C is equal to the high level (+1 V) the switch will be on, and when C is equal to the low level (−1 V) the switch will be off. The J_{-1}, J_0, and J_1 signals are connected to C of the TS that has input y_1, y_2, and y_3, respectively. The value of x determines which TS will be on and, eventually, which signal (y_1, y_2 or y_3) will be displayed at the output.

A ternary full adder has been designed using DECMOS

TABLE III
TRUTH TABLE OF TERNARY FULL ADDER

x	y	c_i	s	c_o
-1	-1	-1	0	-1
-1	-1	0	1	-1
-1	-1	1	-1	0
-1	0	-1	1	-1
-1	0	0	-1	0
-1	0	1	0	0
-1	1	-1	-1	0
-1	1	0	0	0
-1	1	1	1	0
0	-1	-1	1	-1
0	-1	0	-1	0
0	-1	1	0	0
0	0	-1	-1	0
0	0	0	0	0
0	0	1	1	0
0	1	-1	0	0
0	1	0	1	0
0	1	1	-1	1
1	-1	-1	-1	0
1	-1	0	0	0
1	-1	1	1	0
1	0	-1	0	0
1	0	0	1	0
1	0	1	-1	1
1	1	-1	1	0
1	1	0	-1	1
1	1	1	0	1

circuitry described above. The symmetric ternary number system is used in this full adder. The truth table for the sum and carry functions is given in Table III. The full adder is composed of fourteen T-gate circuits. However, a large amount of circuitry can be saved by taking out the J_K arithmetic circuits of all T-gates driven by a single trit and to replace it by a single common J_K arithmetic circuit driving a number of ternary multiplexers (TM), as shown in Fig. 10. Each TM is composed of the set of three TS's of a T-gate. The complete ternary full adder has been simulated successfully on the computer using the SPICE 2G simulation package. The design parameters are given in Section III above.

V. CONCLUSIONS

A new family of ternary logic circuits based on both depletion and enhancement types of complementary MOS transistors (DECMOS) is shown to be useful in the design of ternary digital systems. With the use of voltage power supplies below the transistors threshold voltage and the exclusion of resistors, it is possible to implement this circuitry in VLSI. This new family offers low power consumption, high speed, and comparable performance to the binary counterpart circuitry.

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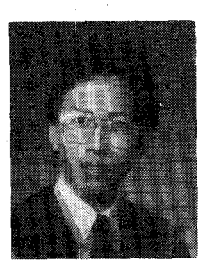

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