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Capricorn (microprocessor)

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The **Capricorn** family of microprocessors was developed by Hewlett-Packard in the late 1970s for the HP series 80 scientific microcomputers. Capricorn was first used in the HP-85 desktop BASIC computer, introduced in January 1980. Steve Wozniak was inspired to build the Apple to be a computer like the HP 9830, and in 1976 he offered HP rights to the Apple computer. He was turned down and was given a release. When the calculator division started an 8 bit computer project called Capricorn, he left for Apple when he wasn't allowed to work on that project.[1][2]

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Architecture [edit]

The Capricorn is a microprogrammed CPU containing 64 eight-bit registers, an eight-bit arithmetic logic unit (ALU), a shifter and control logic. The 64 registers are split by boundaries. There is a boundary every two bytes for the first 32 registers and one boundary per 8 bytes for the remaining 32 registers. Each low-level instruction modifies data beginning at the register addressed up to the next boundary. The design results in very compact code. It was up to the coder to access and modify between one and eight bytes using only one CPU instruction.

The first 32 registers are often used for address manipulation. The remaining 32 registers are used for floating point operations. Because there are four sets of eight byte boundary registers (32-63) most floating point operations are done using only registers without any memory access. Behalf of the first 32 registers one register pair is defined as the program counter, another pair as the stack pointer, and one more pair as an index pointer for internal operations. There is no dedicated accumulator — any general register can be used for ALU results because the register file is designed to allow up to two read and one write operations for the first 32 registers and up to eight read and one write operations for the remaining 32 registers at the same time. Any pair of registers can be used as a 16-bit index register.

The ALU can work either in binary or binary-coded decimal (BCD) mode. Variable-length instructions let the programmer treat data in the upper 32 registers as entities between one and eight bytes in length — for example, two

eight-byte values (e.g. mantissa of a floating-point number) can be added using a single instruction. This feature reduces the number of loops that need to be programmed.

The CPU has an interrupt mechanism with up to 127 vectors. For direct memory access, the CPU can be halted by an external device.

Implementation [edit]

The Capricorn CPU was implemented as a silicon-gate NMOS logic circuit (4.93×4.01 mm) in a 28-pin dual in-line package, with an 8-bit, multiplexed external bus. The CPU chip consumed 330 mW at 625 kHz.

CPU timing is controlled by four non-overlapping clock phases with 200 nanosecond width and 200 nanosecond spacing, for an overall clock cycle of 1.6 microseconds, equivalent to 625 kHz clock frequency.

The complete system included support chips co-designed with the CPU, such as a dynamic memory controller, keyboard controller with timers, printer controller and CRT controller. A special buffer chip connected to the expansion slots.

References [edit]

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- Mikkelsen, Tim. "What is the cpu for HP-87?". Archived from the original on 2009-12-14. Retrieved 2010-02-12.
- "Capricorn CPU documentation (a subset of the HP85 assembler ROM manual)" (PDF). Retrieved 2020-02-06.

Notes [edit]

1. ^ Byte Interview with Steve Wozniak
2. ^ Old Computers HP-85

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